OPTICAL AND ELECTRICAL STUDIES OF SILICON NANOWIRES IN PHOTOVOLTAIC APPLICATIONS

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SUMMARY

Recently, there has been increasing research interest in the application of silicon nanowires (SiNWs) in photovoltaic (PV) cells. SiNW may emerge as a more viable choice over conventional bulk Si structure in future PV devices because of its unique optical and electrical properties. In this work, features and working principles of conventional planar Si solar cell and novel SiNW solar cell have been studied and compared, highlighting the advantages and promising prospect of SiNWs in the design and fabrication of third generation solar cells.

In previous works, SiNWs were fabricated using a variety of methods, which mainly fall into two categories: “bottom-up” growth and “top-down” etching. “Bottom-up” method generally involves Vapour-Liquid-Solid (VLS) growth of crystalline silicon on cheap substrate in the presence of gold or other metal catalysts. “Top-down” method usually refers to etching of starting silicon wafer in ionized plasma (reactive ion etch/plasma etch) or chemical electrolyte (wet etch). Performances of these SiNW based PV devices generally do not exceed 3%, which is significantly lower than that of existing commercial Si solar cells (~20%). This implies that despite the theoretical advantages of SiNWs in solar applications, there exist unsolved technical issues which hinders SiNW PV device from attaining its theoretical efficiency. Therefore, the research emphasis in the community has always been the improvement of device design and experimental techniques, in order to increase the overall power conversion efficiency (PCE) of the devices.

In this work, optical lithography patterned plasma etch was utilised in fabricating highly ordered, vertical SiNWs from single-crystalline Si (100) starting wafer. Several different designs have been explored, including buried p-n junction SiNW solar cell,

buried p-n junction silicon nanowall solar cell and core-shell p-n junction SiNW solar cell. Planar Si control devices have been fabricated as well for comparative analysis. Optical and electrical characterisation demonstrates significant suppression in surface reflection and prominent enhancement of light generated current in SiNW devices. Buried-junction SiNW and nanowall solar cells demonstrate 33% and 42% increase in short circuit current (J_{sc}) comparing to Si planar device, owing to effective light trapping and anti-reflection property of SiNWs. Core-shell SiNW device displays a higher increase of 52% in J_{sc}, as a result of larger junction area from the radial p-n junction. An overall PCE of 8.2% and 4.2% are attained for buried-junction and core-shell junction SiNW devices respectively, surpassing the efficiencies obtained by previous groups with similarly structured SiNW devices. Factors which limit the device performance are also analyzed, revealing the impact of series resistance (R_s) on fill factor (FF) and PCE of the device. Significant improvement of performance could be expected by eliminating the effect of R_s.

In addition, as a promising and highly efficient route of enhancing PCEs in semiconductor PV devices, multiple exciton generation (MEG) has been studied, including its mechanism and experimental detection methods. Photoluminescence (PL) signals from some SiNW samples demonstrate substantial light-emitting property in SiNWs, confirming the validity of time-resolved PL (TRPL) as an effective MEG detection method in SiNWs. Lastly, a proposal of future device design has been raised. The new structure aims at integrating the effect of MEG with buried or core-shell junction SiNW PV device, opening a possibility of further enhancement in PCEs.

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LIST OF SYMBOLS AND ABBREVIATIONS

α	Absorption coefficient
d	Diameter of nanowire
ε	Permittivity
η, η_{PV}	Power conversion efficiency of photovoltaic device
E	Incident photon energy
E_g	Band gap
I	Terminal current
I_0	Dark saturation current
I_L	Light generated current
I_{sc}	Short-circuit current
J_0	Dark saturation current density
J_l, J_G	Light generated current density
J_R	Recombination current density
J_{sc}	Short-circuit current density
K	Boltzmann's constant
L	Length of nanowire
M	Number of exciton pairs generated upon photo-excitation

n	Number of particles
N_A	Acceptor concentration
N_D	Donor concentration
P_{in}	Integrated optical power
q	Electron charge
R_s	Series resistance
t	Time
T	Absolute temperature
V	Terminal voltage
V_{bi}	Built-in voltage
$V_{junction}$	Voltage across p-n junction
V_{oc}	Open-circuit voltage
“AR”	Auger Recombination
“BOE”	Buffered Oxide Etch
“DSSC”	Dye-Sensitised Solar Cell
“FF”	Fill Factor
“II”	Impact Ionisation
“MEG”	Multiple Exciton Generation

“NC”	Nanocrystal
“PL”	Photoluminescence
“PV”	Photovoltaic
“PCE”	Power Conversion Efficiency
“QD”	Quantum Dot
“QY”	Quantum Yield
“SEM”	Scanning Electron Microscopy
“SiNC”	Silicon Nanocrystal
“SiNT”	Silicon Nanotip
“SiNW”	Silicon Nanowire
“SiNWall”	Silicon Nanowall
“SiNWire”	Silicon Nanowire
“SPM”	Sulphuric Acid-Hydrogen Peroxide Mixture
“TA”	Transient Absorption
“TCSPC”	Time-correlated Single Photon Counting
“TEM”	Transmission Electron Microscopy
“TRPL”	Time-resolved Photoluminescence
“VLS”	Vapour-Liquid-Solid

CHAPTER 1

INTRODUCTION

1.1 Development of silicon photovoltaic devices

The search for energy supplies has always been one of the most important quests for generations. In the light of recent events such as diminishing fossil fuel supplies, surge in oil prices and an increasing awareness of effect of greenhouse gases such as carbon dioxide on the global climate [1], the necessity of finding and utilising clean, renewable energy sources is of paramount importance to humanity.

Being clean, renewable and universally abundant, solar energy seems to be the most viable choice to meet our energy demand [2]. The sun delivers continuously to earth 120,000 TW of energy, which dramatically exceeds our current rate of energy consumption (13 TW) [3]. Solar energy can be captured as heat through many types of absorber materials, or converted into electricity using photovoltaic (PV) materials.

Semiconductor PV devices have been under research for more than 100 years, exploring a variety of materials. This project will focus on devices fabricated using silicon, which is the most abundant and widely used semiconductor PV material today.

Three generations of devices have been developed, each with its advantages and limitations. Their development and prominent properties are presented briefly in Chapter 2.

1.2 Integration of silicon nanowires into PV devices

There has been increasing research interests in deploying nanostructures, silicon nanowires (SiNWs) in particular, into the third generation devices, as the novel

properties of these structures present exciting possibilities for future improvement on the device performances.

The optical and electrical properties of SiNWs are reviewed in Chapter 3. In comparison to bulk Si, SiNWs have exhibited potentials for enhancement of power conversion efficiencies (PCEs) and reduction of manufacturing cost in future PV device fabrications, making them a newly emerged area of the research interest.

been shown to exhibit potential advantages in application to PV device fabrications, addressing issues such as enhancement of power conversion efficiencies (PCEs) and reduction of manufacturing cost, Recent theoretical and experimental works carried out by various groups will also be presented and discussed.

1.3 Multiple exciton generation

The PCE for single junction Si crystalline PV cell is limited to about 33% under standard AM1.5 solar spectrum [7]. About 47% of the incident solar power is lost through the process of thermalisation, in which the excess energy of carriers generated by absorption of supra-band gap photons is converted to heat [4]. The conception and fabrication of PV devices that may exceed the Shockley-Queisser efficiency limit has been of increasing research interest in the past decade. Multiple exciton generation (MEG) has been considered as a mechanism to utilise some of the excess energy of photogenerated carriers to create additional electron-hole pairs per incident photon, thus increasing the quantum yield and PCEs of PV devices.

The mechanism of MEG is presented in Chapter 4, which will consequently demonstrate the possibility of enhancing the PCEs of PV devices beyond the Shockley-Queisser limit through a detailed balance model.

As the focus in this project is the design and fabrication of a highly efficient SiNW PV device, MEG may serve as an effective route for significant improvement of PCEs. However, as no MEG in one dimensional SiNW PV devices has been reported, experimental studies of MEG in zero dimensional Si nanocrystals (SiNCs) done by previous groups become highly relevant and useful as a reference for our future MEG detection in SiNWs. These works will also be discussed in Chapter 4, including MEG detection methods and experimental results.

1.4 Experimental studies

1.4.1 Buried-junction silicon nanowire (SiNWire) and silicon nanowall (SiNWall) solar cell

Design and fabrication of buried-junction SiNWire and SiNWall solar cell is discussed in Chapter 5. Optical reflectance measurement demonstrates a drastic suppression in total reflection, confirming excellent anti-reflection property of silicon nanostructures. I-V data obtained under standard AM 1.5 G illumination is presented and analysed, showing that the enhanced light absorption leads to larger light generated current and higher PCE in solar cells with surface nanostructures as compared to planar Si solar cell.

1.4.2 Core-shell SiNW solar cell

SiNW solar cells with core-shell radial p-n junction is subsequently designed and fabricated, in order to exploit the orthorgonalisation of light absorption and carrier collection. Ion implantation method was explored in order to achieve a shallow and highly doped radial p-n junction. The process and analysis is demonstrated in Chapter 6. Beside similar reduction in light reflection as observed in buried junction SiNW

solar cell, core-shell SiNW solar cell demonstrate significantly higher increase in light generated current as compared to Si planar control device, owing to higher junction area and more efficient carrier generation-collection process in radial p-n junction.

1.4.3 SiNW array for MEG test

This experiment is a preliminary study of the possibility of integrating MEG into the carrier generation mechanism of SiNW PV devices. It aims at fabricating an array of ultra-thin SiNWs in which MEG phenomenon could be detected. In Chapter 7, the fabricating and sharpening process of this SiNW array is described. Photoluminescence (PL) spectroscopy measurements of some samples were performed, and the results are presented and discussed. This PL measurement verifies the existence of significantly strong PL signal in one-dimensional SiNWs arrays, and serves as a stepping stone for MEG detection by time-resolved photoluminescence (TRPL) in future studies.

1.4.4 Future device design

Based on literature review and experimental studies on SiNW device fabrication and performance, a new device structure has been proposed in Chapter 8. This structure could be capable of combining the advantages of traditional planar single junction crystalline Si PV device and of SiNWs, such as anti-reflection property and MEG. Also, existing technical difficulties and possible solutions are discussed, highlighting the challenges to be confronted in future studies.

CHAPTER 2

THREE GENERATIONS OF SILICON PHOTOVOLTAIC DEVICES

2.1 First generation

First generation devices consist of large-area, high quality and single junction crystalline silicon PV cells, which still comprises more than 90% of all photovoltaic cell production today [4]. This could be attributed to several reasons. Firstly, silicon is a readily available, nontoxic material which can be refined into extremely pure form with high electron and hole mobilities. Secondly, silicon is readily doped to achieve high electron and hole concentrations, which allows efficient carrier separation and low resistance contacts to be made [1]. Lastly, single junction silicon photovoltaics could attain relatively high power conversion efficiencies (25% for laboratory best and 23%-24% for the best commercial cells based on single-crystal silicon [3]).

However, these devices suffer from several drawbacks. Silicon has relatively low absorption coefficient, especially in the near-infrared region (4.65×10^{1} cm^{-1} at 1000 nm), thus requiring substantial absorber layers to improve light absorption [1]. Extremely pure and highly ordered materials are necessary to minimise carrier recombination and facilitate efficient carrier collection in thick devices, as low minority carrier diffusion lengths result from high level of impurities or high density of defects [5]. Therefore, inexpensive materials with low diffusion lengths and low absorption coefficients cannot be readily incorporated into first generation solar-cell structures with high energy conversion efficiencies [6]. As a result, extra cost of purification is incurred.

Therefore, research interests have arisen to reduce manufacturing and installation cost, while achieving high efficiencies in the next generations of PV devices.

2.2 Second generation

Second generation devices are developed utilising technologies such as vapour deposition and electroplating to deposit a thin film of semiconductor materials such as cadmium telluride (CdTe), copper indium gallium selenide ($CuInGaSe_2$) and amorphous silicon on a supporting substrate such as glass and ceramics, reducing the material mass and therefore cost [8]. However, the challenge of improving their efficiencies remains [2].

By exploring the possibility of absorption enhancement with different types of materials, several other types of devices have also been fabricated, such as dye-sensitised solar cells (DSSCs), bulk heterojunction cells and organic cells, which provide promising prospect of inexpensive and large-scale solar energy conversion. However, the PCEs achieved are not satisfactory, with laboratory DSSCs based on cheap organic materials being only 2-5% efficient [2].

2.3 Third generation

Third generation PV cells aim to enhance electrical performance beyond the Shockley-Queisser limit while maintaining low production cost. This possibility has been explored by research of MEG in semiconductor nanocrystals (NCs). At theoretical level, total PCE in NCs could be increased to up to 45% by MEG [11]. In experimental studies, although MEG has been observed in a variety of NCs, an effective technical method for harvesting the additional carrier pairs is yet to be formulated [4, 22-26].

Recently, there has been increasing research interests in deploying nanostructures into silicon PV devices, as the novel optical and electrical properties of these structures present exciting possibilities for future improvement on the device performances.

CHAPTER 3

SILICON NANOWIRE PHOTOVOLTAIC DEVICES

3.1 Potential advantages

Silicon nanowires (SiNWs) present several advantages over bulk Si in PV applications due to their unique optical, electric and electronic properties.

The primary advantage is the decoupling of absorption length and carrier collection, in contrary to bulk Si PV cells. A radial p-n junction nanowire oriented toward the illumination source could be long in the direction of incident light, presenting a large-cross section which allows optimal light absorption. Meanwhile, the nanowire could be thin in the radial direction, allowing short distance for effective carrier collection [1, 9]. The substantial anti-reflection effect of nanowire arrays [10] also renders their application to PV devices more desirable.

A detailed balance model used by Hanna and Nozik [11] has shown that the optimum band gap for PV materials is approximately 1.4 eV, which corresponds to the Shockley-Queisser limit of maximum single junction power conversion efficiency at the standard AM 1.5G solar spectrum. Theory and experiment has shown that for SiNWs, the band gap could be tuned to 1.4 eV when the nanowire diameter is approximately 3.5 nm [12].

In addition, organic dyes could be adsorbed onto the surface of the SiNW array, allowing sensitisation of the material to other regions of the solar spectrum by carrier or energy transfer [1].

3.2 Optical properties

Theoretical studies on the optical properties of SiNWs have been carried out by Hu and Chen [13]. It was found that for a square array consisting for SiNWs with 50, 65 and 80 nm diameters and a constant separation of 100 nm, substantial absorption was only observed at energies above 2.5 eV (500 nm) for an absorption length of 4.66 μm. Increasing fill ratio (by increasing nanowire diameter) from 0.2 to 0.5 reduced to onset of absorption to approximately 2.0 eV (620 nm).

Optical properties of SiNWs investigated by experimentations vary slightly from the theoretical results. According to Tsakalakos *et al.* [14], two types of nanowires prepared by different methods display comparable optical absorption properties. The first type was a vertical SiNW array with nanowire diameter between 20 and 100 nm, produced by chemical etching using $AgNO_3$ and HF (Fig. 1(a)). Strong light absorption and excellent anti-reflection property was observed between 300 and 800 nm, while there is also approximately 20% absorption between 1100 and 1900 nm. The below-band-gap absorption has been explained by strong IR light trapping and presence of surface states on the nanowires [1].

The second type was produced by vapour-liquid-solid (VLS) growth on glass substrate, resulting in randomly oriented nanowires (Fig. 1(b)). Strong absorption (>50%) was shown over the entire visible and near-IR regions from 200-2000 nm [14]. The substantial absorption below the band gap of silicon may be attributed to the tangled geometry of the array, but additional study is still required [1].

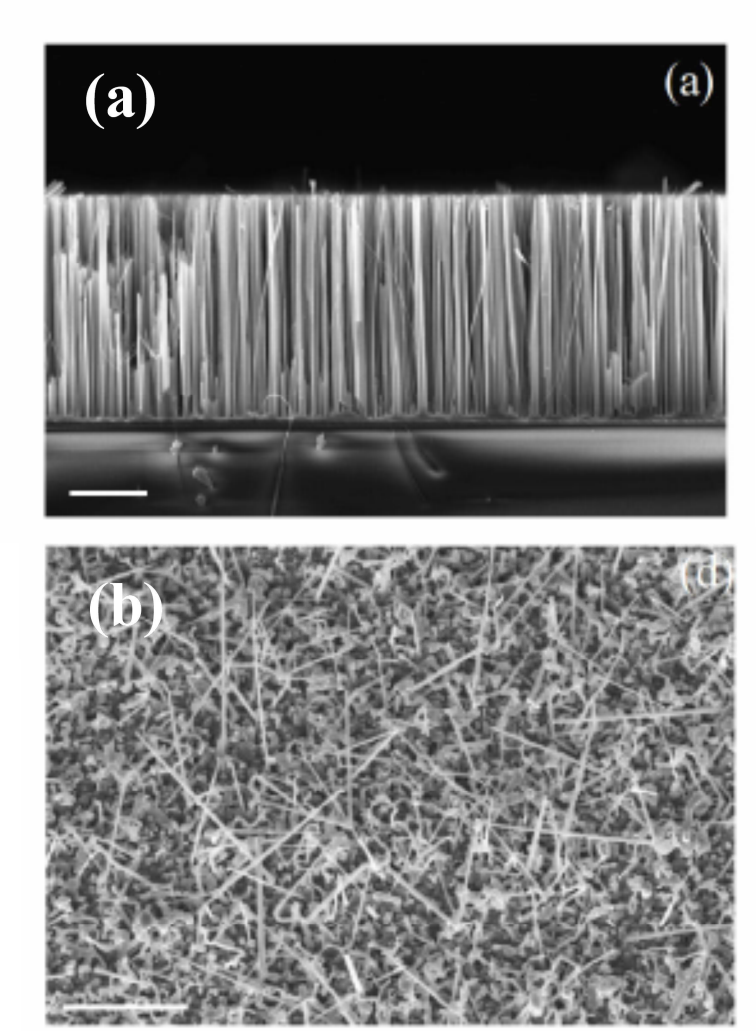

Fig. 1. (a) Scanning Electron Microscopy (SEM) cross-section image of 10 µm thick vertically aligned SiNW array produced by etching. (b) SEM image (30° tilt) of randomly oriented SiNWs produced by VLS growth (Produced from Ref. [14]).

3.3 Electrical properties

Two cases were considered to study the physics of charge generation, separation and transport in nanowires: axial and radial p-n junction.

3.3.1 Axial p-n junction

This type of nanowire has the p-n junction along its axis such that the n-type and p-type regions are located at each end of the nanowire respectively (Fig. 2). It was found by Zervos through a self consistent calculation using the Schrodinger and Poisson equations [15] that a depletion region forms along the surface of the p and n type regions, whose depth depends on the doping level and the wire diameter. At the p-n junction somewhere along the length of the nanowire, the depletion width is found to be 3 times wider than that of the planar p-n junction with the same material and doping level. In addition, the built-in voltage at the p-n junction decreases with reducing wire diameter. Therefore, it would be desirable to keep the nanowire diameters large in order to ensure sufficient charge transport in competition with the surface depletion effect.

However, the total p-n junction is small, which equals only to the cross-sectional area of the nanowires [1]. This significantly limits the possibility of more efficient charge separation in nanowires with axial p-n junction.

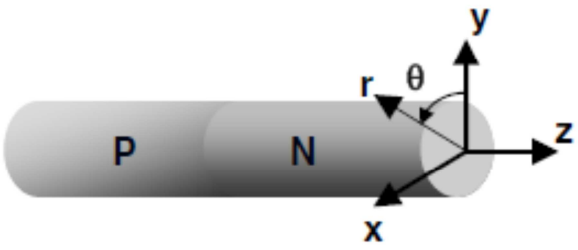

Fig. 2. Schematic demonstration of a nanowire with built-in axial p-n junction (Produced from Ref. [15]).

3.3.2 Radial p-n junction

A core-shell structure of nanowire array on a conductive substrate was proposed and examined by Kayes *et al.* (Fig. 3) [9]. With the p-n junction now in the radial direction, the junction area is expanded drastically compared to a planar or axial p-n junction nanowire device.

The most prominent feature of such a structure is the decoupling of charge generation by light absorption in the axial direction from charge separation and transport in the radial direction, as mentioned earlier (*See Section 3.1*). Nevertheless, it was emphasised that in order to achieve significant improvement in power conversion efficiencies compared to convention bulk Si solar cells, two conditions must be satisfied [9]. Firstly, the device should be designed such that the minority carrier diffusion length is short compared to the penetrating depth of the absorber. As a result, the optimum radius of the nanowires should be equal to the minority carrier diffusion length, which should be very small compared to the optical thickness of Si. Secondly, the rate of carrier recombination in the depletion region must not be too large, which implies that for silicon, the carrier lifetimes in the depletion region must be longer than 10 ns.

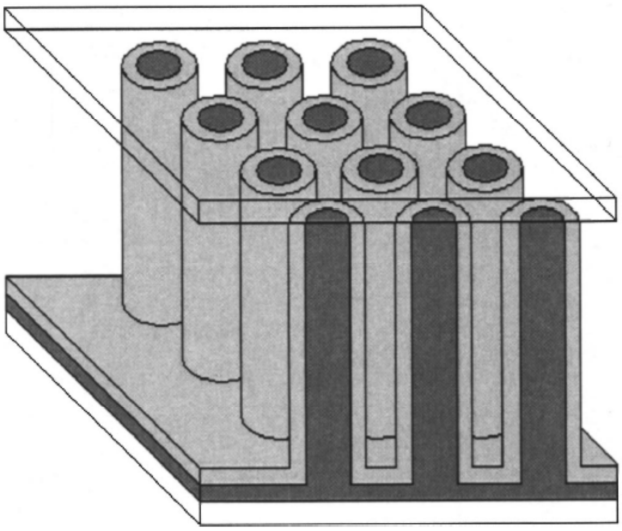

Fig. 3. Schematic cross-section of the radial p-n junction nanowire cell. Light is incident on the top surface. The light grey area is n type, the dark grey area p type (Produced from Ref. [9]).

A mathematical model involving the solution of diffusion and drift equations for minority carriers, current continuity equations and Poisson's equation in the geometry of interest was deployed by B. M. Kayes et al. to examine the electrical and electronic properties [9]. Cell performance was assessed based under the variation of parameters such as the SiNW length, radius and core-shell doping levels and trap density of the material.

It was found that there exists an optimum wire length for which the power conversion efficiency (PCE) attains a maximum. This could be qualitatively explained by analysing the competing effect of light generated current density (J_l) and dark saturation current density (J_0), both increasing with the nanowire length (L):

$$\boldsymbol{J_l \propto (1 - e^{-\alpha L})}, \quad \boldsymbol{J_0 \propto L}. \qquad \text{(Eq. 1)}$$

α is the absorption coefficient, which is wave-length dependent.

The short-circuit current density (J_{sc}) was found to be independent of the trap density in the cell, in contrast to planar cells where J_{sc} falls rapidly with increasing trap density. The open-circuit voltage (V_{oc}) decreases significantly with nanowire diameter if the trap density in the depletion region is high, but is almost independent of the trap density in the quasi-neutral region [9]. Combining these factors, it was concluded that while planar cells have low efficiency when there is high trap density anywhere in the cell, radial p-n junction nanowire cell efficiency remains high despite a high quasi-neutral region trap density provided that the depletion region trap density remains low. This theoretical study implies that SiNW solar cells are much less sensitive to impurities compared to planar Si solar cells.

3.4 Device fabrication and performance

Semiconductor nanowire devices in recent years have been predominantly fabricated using silicon because single-crystal nanowires are easily produced using techniques such as vapour phase VLS growth [14, 16, 17, 19, 20] or etching of crystalline wafers [10, 18].

Both single SiNW [19, 20] and SiNW arrays [16-18, 21] have been fabricated and their photovoltaic properties measured. The works of various groups are summarised in Table 1 and 2. All the measurements were taken under the standard AM 1.5G illumination.

Table 1. Summary of recent advances on SiNW device fabrication.

Author & year	**SiNW structure**	**Dia. (nm)**	**Fabrication method**
Tian et al., 2007	Single p(core)-i-n(shell)	300	**NW**: VLS growth **Contact**: litho defined etching and metal deposition
Kelzenberg et al., 2008	Single n-type	900	**NW**: VLS growth **Contact**: Al rectifying junction by photolithography with evaporated Al lines
Tsakalakos et al., 2007	Array p(core)-n(shell)	109±30	**Core**: VLS growth **Shell**: PECVD (a-Si), sputter coat (transparent ITO) **Contact**: Al finger by evaporation
Stelzner et al., 2008	Array n-type NW on p-type wafer	20-100	**NW**: VLS growth. Doped during growth with PH_3 or B_2H_6
Peng et al., 2008	Array n-type	20-300	**NW**: HF/$AgNO_3$ or HF/H_2O_2 wet etch **Contact**: electrolyte with HBr/Br_2
Garnette & Yang, 2008	Array n(core)-p(shell)	350-400	**Core**: HF/$AgNO_3$ wet etch **Shell**: LPCVD (a-Si) with RTA **Contact**: sputtered Ti/Ag on n-Si and Ti/Pd on p-Si

Table 2. Summary of recent advances on SiNW device PV measurements.

Author & year	SiNW structure	Dia. (nm)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	PCE (%)
Tian et al., 2007	Single p(core)-i-n(shell)	300	0.503 nA*	0.26	55	3
Kelzenberg et al., 2008	Single n-type	900	5.0	0.19	40	0.46
Tsakalakos et al., 2007	Array p(core)-n(shell)	109±30	1.7	0.13	28	0.1
Stelzner et al., 2008	Array n-type NW on p-type wafer	20-100	2	0.23 – 0.28	20	0.1
Peng et al., 2008	Array n-type	20-300	0.87	0.73	-	-
Garnette & Yang, 2008	Array n(core)-p(shell)	350-400	4.28	0.29	33	0.46

* I_{sc} of single nanowire solar cell

3.5 Discussion

Evident from the measurements above, the performances of SiNW solar cells are as yet unsatisfactory, although single-nanowire devices have demonstrated better efficiencies. The following factors could have impacted the PV properties:

Un-optimised nanowire dimensions and geometries

The length of the SiNWs should be sufficiently long for full light absorption, and the mean nanowire radius should be optimised to be approximately equal to the mean minority carrier diffusion length in the nanowires [9, 17]. The depletion region must be kept small so that the nanowires are not fully depleted, thus requiring a sufficiently

high doping level. For an estimated doping level of 10^{18} cm^{-3} [17], the expected depletion width is approximately 50 nm. The un-optimised nanowire diameters could provide a partial explanation to the low V_{oc} measured. The poor nanowire density and alignment [17] could have also impacted the optical absorption property of the device.

Au as the catalyst for VLS growth

Since gold is typically used for VLS growth of SiNWs, there will be some recombination centres in wires produced by this process that are determined by solubility of gold at the deposition temperature [1, 17].

Surface recombination

The large surface roughness observed in etched SiNWs could lead to enhanced depletion region traps, especially since this surface is located directly at the p-n junction of the final device. Further optimisation through surface passivation could yield better efficiencies [21].

CHAPTER 4

MULTIPLE EXCITON GENERATION

4.1 Mechanism

MEG per photon is realised through the mechanism of impact ionisation (II), in which a high-energy exciton created by absorbing a photon with energy greater than two times of the absorption threshold (band gap E_g), relaxes to the band edge via energy transfer of at least $1E_g$ to a valence band electron, which is excited above the energy gap (Fig. 4(a)) [22].

The multiple excitons generated through II could subsequently go through several relaxation paths, such as inelastic carrier-carrier scattering, phonon scattering, exciton-exciton annihilation and Auger recombination (AR).

AR is the inverse of II, whereby an exciton recombines via energy transfer to an electron or hole that is excited to a higher energy state (Fig. 4(b)) [22].

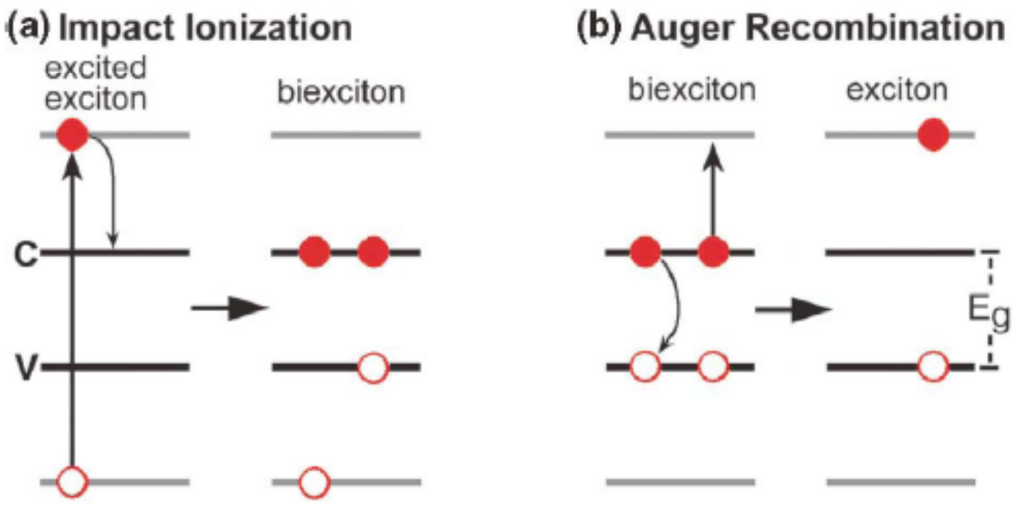

Fig. 4. (a) Impact ionisation and (b) Auger recombination process. Electrons (filled red circles), holes (empty red circles), conduction band (labelled C) and valence band (labelled V) (Produced from Ref. [22]).

4.2 MEG in bulk vs. in quantum-confined semiconductors

In existing PV devices, MEG has not contributed meaningfully to improve the quantum yield. Impact ionisation is not likely to occur with significant efficiency in bulk semiconductors, because the threshold photon energy for II exceeds the requirement for the energy and crystal momentum conservation. In addition, the rate of II is slow versus of rate of energy relaxation by electron-phonon scattering, which is very fast (sub-ps) in bulk semiconductors [23].

However, MEG could be greatly enhanced in semiconductor quantum dots (QDs) (or nanocrystals (NCs)), as the threshold photon energy for II is lowered due to the relaxation of momentum conservation constraint. Moreover, the rate of electron

relaxation through electron-phonon interactions is largely reduced because of the discrete character of the electron-hole spectra.

While Auger recombination is insignificant in bulk material due to energy and momentum conservation constraints, it becomes efficient in QDs due to the enhanced Coulomb interaction between excitons and relaxation of momentum conservation [22].

4.3 Calculation of power conversion efficiencies

4.3.1 Detailed balance model

A detailed balance model was established by Hanna and Nozik [11] to calculate the maximum power conversion efficiencies in single gap PV devices, with the effect of MEG. The current versus voltage dependence at any operating point is written as:

$$\boldsymbol{J(V, E_g) = J_G(E_g) - J_R(V, E_g)}\,, \qquad \text{(Eq. 2)}$$

J_G and J_R, being the photogenerated current and the recombination current respectively, are dependent on voltage and quantum yield (QY).

QY as a function of incident photon energy (*E*), is modelled by a sum of step functions for ideal MEG QD absorbers:

$$\boldsymbol{QY(E) = \sum_{m=1}^{M} \theta(E, mE_g)}\,, \qquad \text{(Eq. 3)}$$

$\theta(E, mE_g)$ is the Heaviside unit step function, and *M* is the number electron-hole pair generated.

At a given operating point (*J*, *V*), the photovoltaic PCE is given by:

$$\boldsymbol{\eta_{PV}(V) = J(V)V/P_{in}}\,, \qquad \text{(Eq. 4)}$$

P_{in} is the integrated optical power in the AM 1.5G spectrum. The maximum PCE with a given absorption threshold E_g and QY can be found by maximising η_{PV} with respect to the operating voltage *V*.

4.3.2 Results

It was found that the maximal power conversion efficiency increases with M and with solar concentration (Fig. 5).

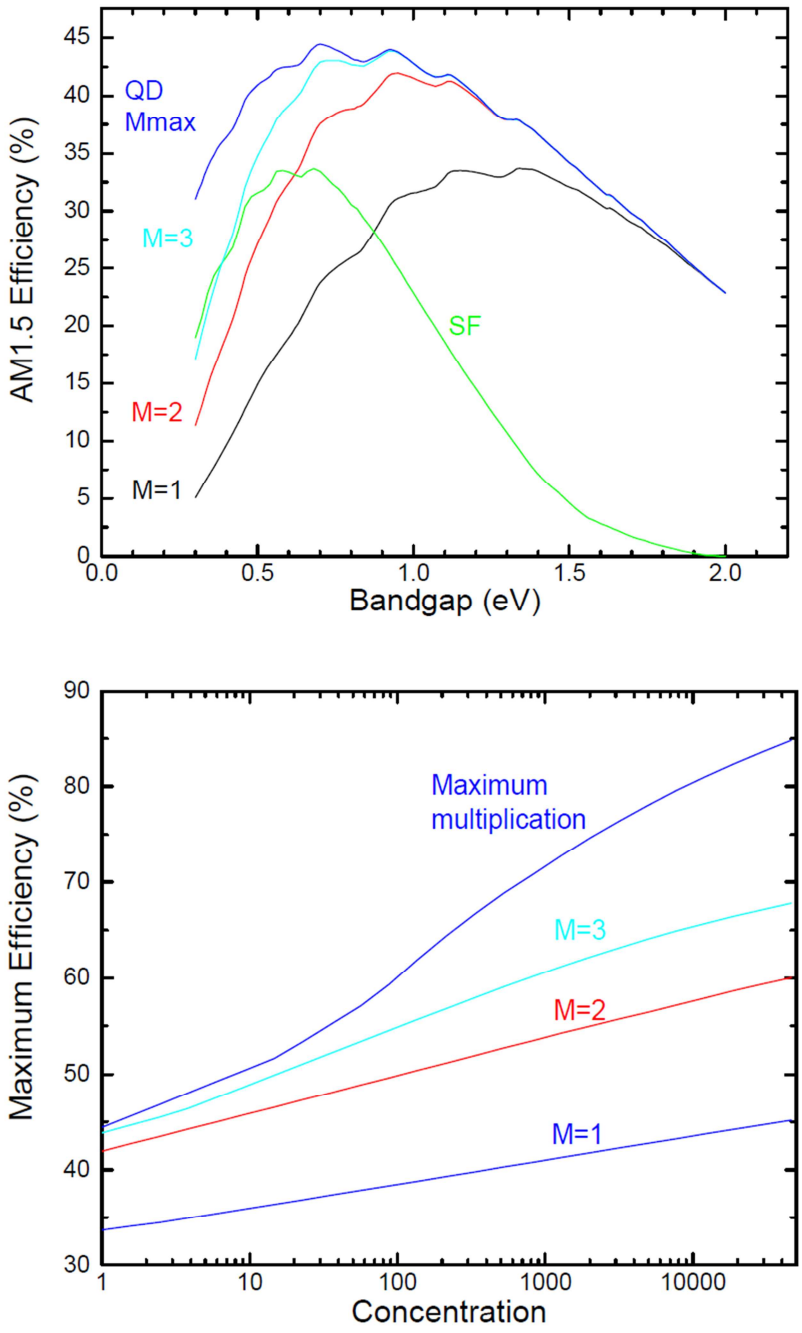

Fig. 5. Dependence of PCE limit on *M* (top) and solar concentration (bottom) for single gap devices. QD M_{max} refers to the maximum multiplication of carrier pairs generated in quantum dots. SF refers to the cell surface sensitised with sulphur fluoride chromophore absorber (Produced from Ref. [11]).

The curve labelled M = 1 has no MEG and corresponds to the Shockley-Queisser limit with a maximum PCE of 33.7% occurring at E_g = 1.34 eV. The maximum efficiency is 44.4% for E_g = 0.7 eV, with M_{max} = 6. Meanwhile, it should be remarked that a high efficiency of 41.9% is obtained with M = 2, occurring at E_g = 0.95 eV. This shows that significant improvement on PCE could be possibly attained with a carrier multiplication of only 2.

4.4 Detection methods

Quantum efficiencies exceeding unity by MEG was achieved by "defect-engineering" in bulk Si in 1993 [47]. More recently, MEG has been detected and studied in PbSe, PbS [22-24], CdSe [25], InAs [26] and Si NCs [4], mainly by the following two techniques: transient absorption (TA) spectroscopy [4, 23-28] and time-resolved photoluminescence (TRPL) [26, 28-32].

4.4.1 Transient absorption spectroscopy

As MEG is a process in which highly excited excitons are converted to biexcitons, transient absorption spectroscopy is able detect MEG via distinguishing between the relaxation dynamics of these two species. Specifically, single excitons recombine slowly with a sub-microsecond time constant, biexcitons recombine rapidly via AR in a picoseconds time scale (Fig. 6).

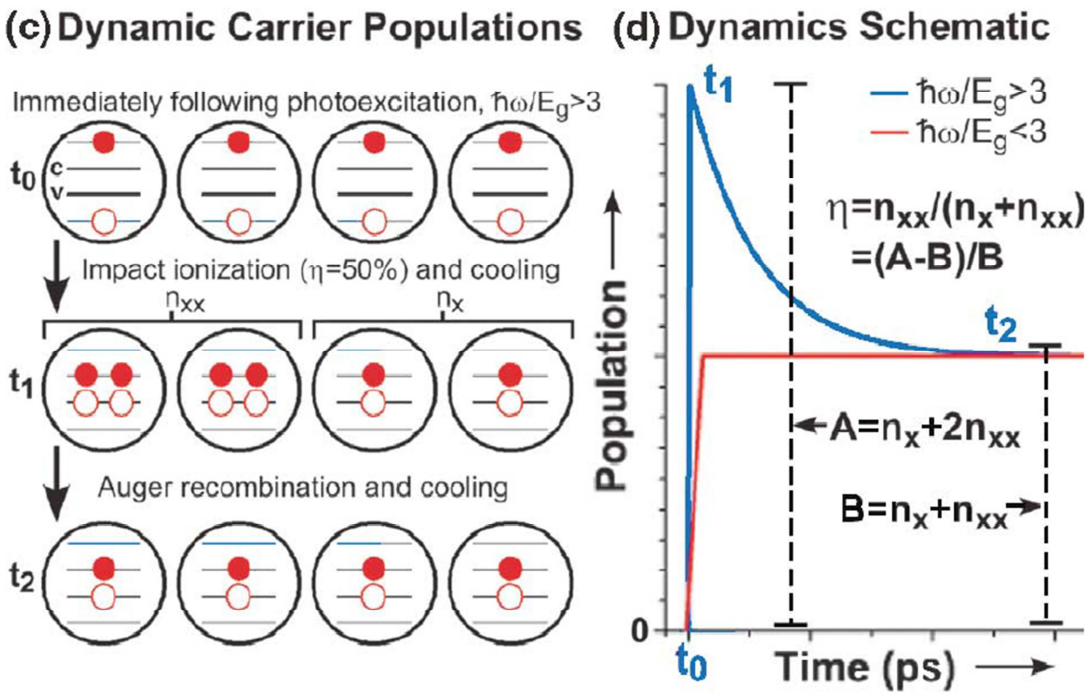

Fig. 6. Difference in single exciton and biexciton relaxation dynamics. The fast component in the blue trace is characteristic of the AR in biexcitons (Produced from Ref. [23]).

For TA spectroscopy, a femtosecond laser system is used to produce pump and probe laser pulses [24, 26]. The pump pulse is tuned to be above the absorption threshold E_g to generate excitons, while the probe pulse is tuned to E_g. After excitation, probe pulse is used to monitor the exciton population versus time.

The NCs are first excited at low pump photon energies (< $2E_g$), at which MEG is not possible. When pump intensity is low, only single photon is absorbed and single exciton formed per NC, displaying a typical slow single-exciton radiative decay dynamics. While introducing high pump intensity, each NC is able to absorb two photons and forms a biexciton, which undergoes rapid AR process.

Subsequently, the NCs are excited at high pump photon energies (> $2E_g$) and low intensity, such that each NC only absorbs one photon but MEG is enabled. If the decay dynamics registered is consistent with the AR of biexcitons observed earlier, MEG is indicated.

Despite being a widely used and reliable technique for MEG detection, TA suffers from a number of limitations [26], such as the requirement for a complex and expensive amplified laser system, unsuitability for in-direct gap materials with no distinct bleaching features and for materials with multi exciton lifetimes.

4.4.2 Time-resolved photoluminescence spectroscopy

In time-resolved photoluminescence (PL), NCs are excited by 100 fs pulses derived from a 250 kHz amplified Ti:sapphire laser with photon energy below (to disable MEG) and then above the absorption threshold E_g (MEG possible). PL lifetimes are measured by multichannel plate detector and time-correlated single photon counting (TCSPC) electronics.

Time dependence of PL from the excited NCs is monitored via TCSPC electronics. A fast decay component due to AR of biexcitons is observed, which provides a dynamic signature of MEG. The result is shown to be coherent with that obtained from TA (Fig. 7(a)).

In addition, biexcitons exhibit enhanced exciton-exciton interaction energies Δ_{XX} relative to the bulk, due to the attractive interactions between two excitons in a spherical NC. The emission spectrum of biexciton is red-shifted relative to that of a single exciton (Fig. 7(b)) [26]. This serves as a spectral signature of MEG, which is an additional feature of time-resolved PL.

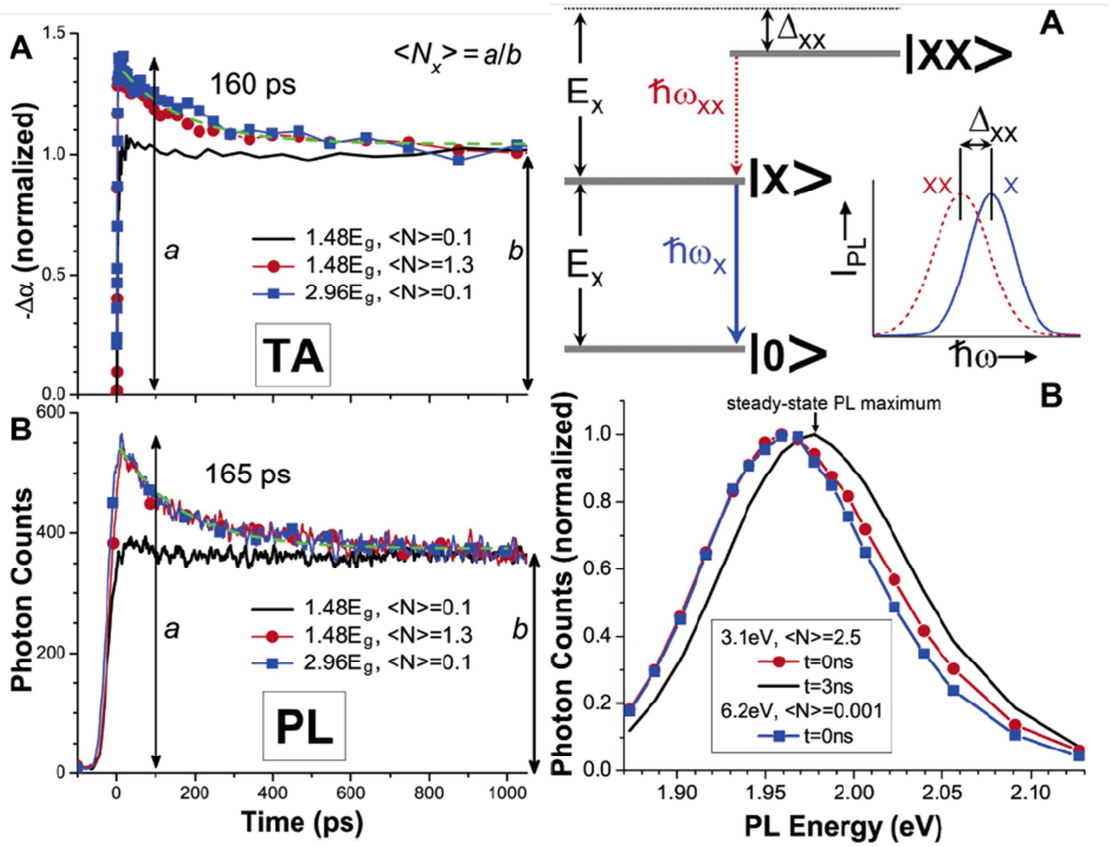

Fig. 7. (a. Left) Dynamic signature of MEG by TRPL and comparison with TA. (b. Right) Spectral signature of MEG by TRPL. The red-shift from the steady state PL maximum is a result of the enhanced exciton-exciton interaction energy Δ_{XX} (Produced from Ref. [26]).

TRPL offers a number of advantages in MEG studies compared to TA, including, for example, higher sensitivity, simplicity and availability with regard to instrumentation in the context in this project. Therefore, PL measurement will be employed in the experimental works in this project.

4.5 MEG studies in SiNCs by photoluminescence

Considering its relative simplicity [26], photoluminescence (PL) spectroscopy has been employed in numerous experimental studies of photoelectric properties of Si

nanostructures. PL is weak in bulk Si because of the long radiative lifetime (millisecond) which could not compete with faster nonradiatve recombination routes. However, quantum confinement and spatial localisation of excited carrier pairs in Si nanocrystals (NCs) or quantum dots (QDs) could push up the radiative efficiency to values as high as 10-50% [31]. As a result, time-resolved PL decay dynamics are mostly observed in quantum confined regions such as SiNCs rather than in bulk Si.

The focus in this project is the design and fabrication of a highly efficient Si nanowire (SiNW) photovoltaic (PV) device, in which multi-exciton generation (MEG) may serve as an effective route of improving the power conversion efficiency (PCE) significantly. However, as no MEG in one dimensional SiNW PV devices has been reported, experimental result of MEG detection by time-resolved PL in zero dimensional SiNCs becomes highly relevant and useful as a reference for our future MEG detection in SiNWs.

In recent years, time-resolved PL decay dynamics has been detected by various groups, in SiNCs embedded in dielectric environment such as SiO_2 [27-30]. Two types of decay have been observed: a slow component (with a microsecond time constant) which corresponds with single exciton recombination, and a fast component (with a picoseconds time constant) which corresponds with biexciton Auger decay [4, 28] and could be a dynamic signature of MEG. According to the work of Trojánek *et al.* [28], these two components exhibit distinctive spectral and temporal characteristics under the excitation wavelength of 532 nm.

4.5.1 Spectral response

The spectra of the fast and slow component of PL decay are shown in Fig. 8. The PL peak of the slow component corresponds with the band gap of the SiNCs studied

(approximately 740 nm). The spectrum of the fast component is very broad, ranging from 350 nm to 850 nm.

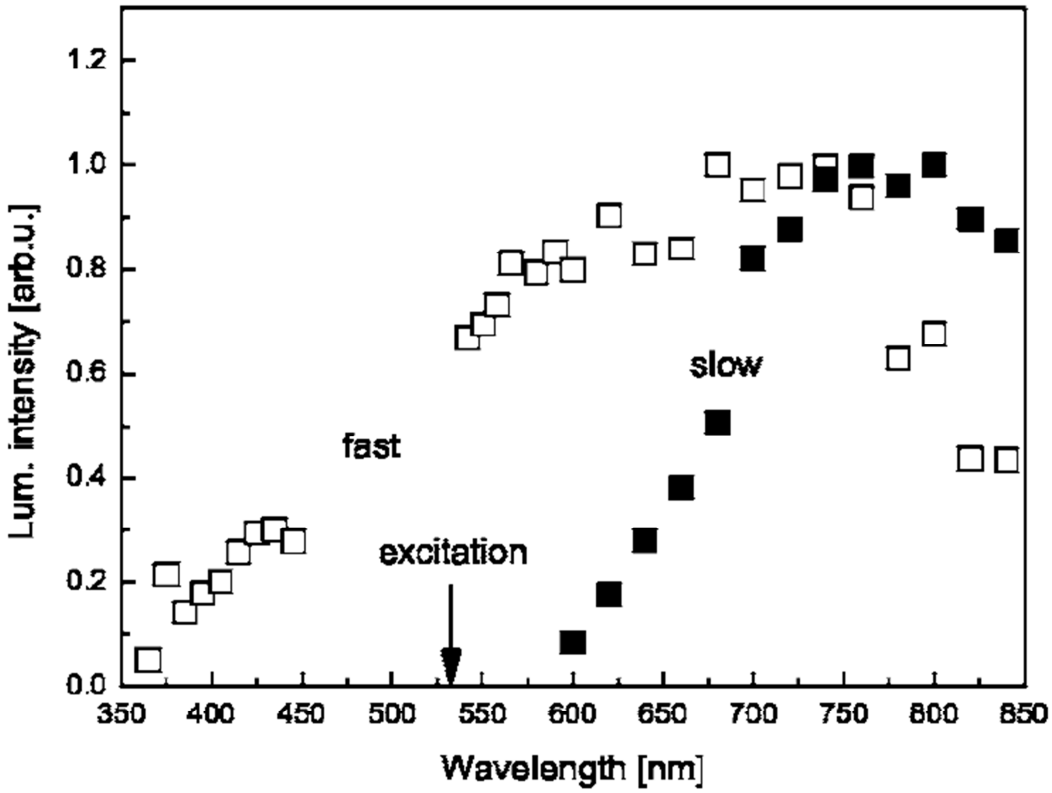

Fig. 8. Spectra of the fast and slow components of PL decay (Produced from Ref. [28]

In addition, it was found that the PL amplitude of the slow component depends linearly on pump fluence with saturation at high fluences. On the other hand, the PL amplitude of the fast component displays quadratic dependence on pump fluence within its entire spectrum (Fig. 9(b) inset). This quadratic dependence is an indication of the fact that PL originates in NCs containing two carrier pairs [28].

4.5.2 Temporal response

As illustrated in Fig. 9(a), the slow component of PL decay could be fitted well by a stretched-exponential function:

$$\boldsymbol{I_{PL} = \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]}, \qquad \text{(Eq. 5)}$$

The parameters τ and β vary with the PL wavelength as shown in the inset of Fig. 9(a).

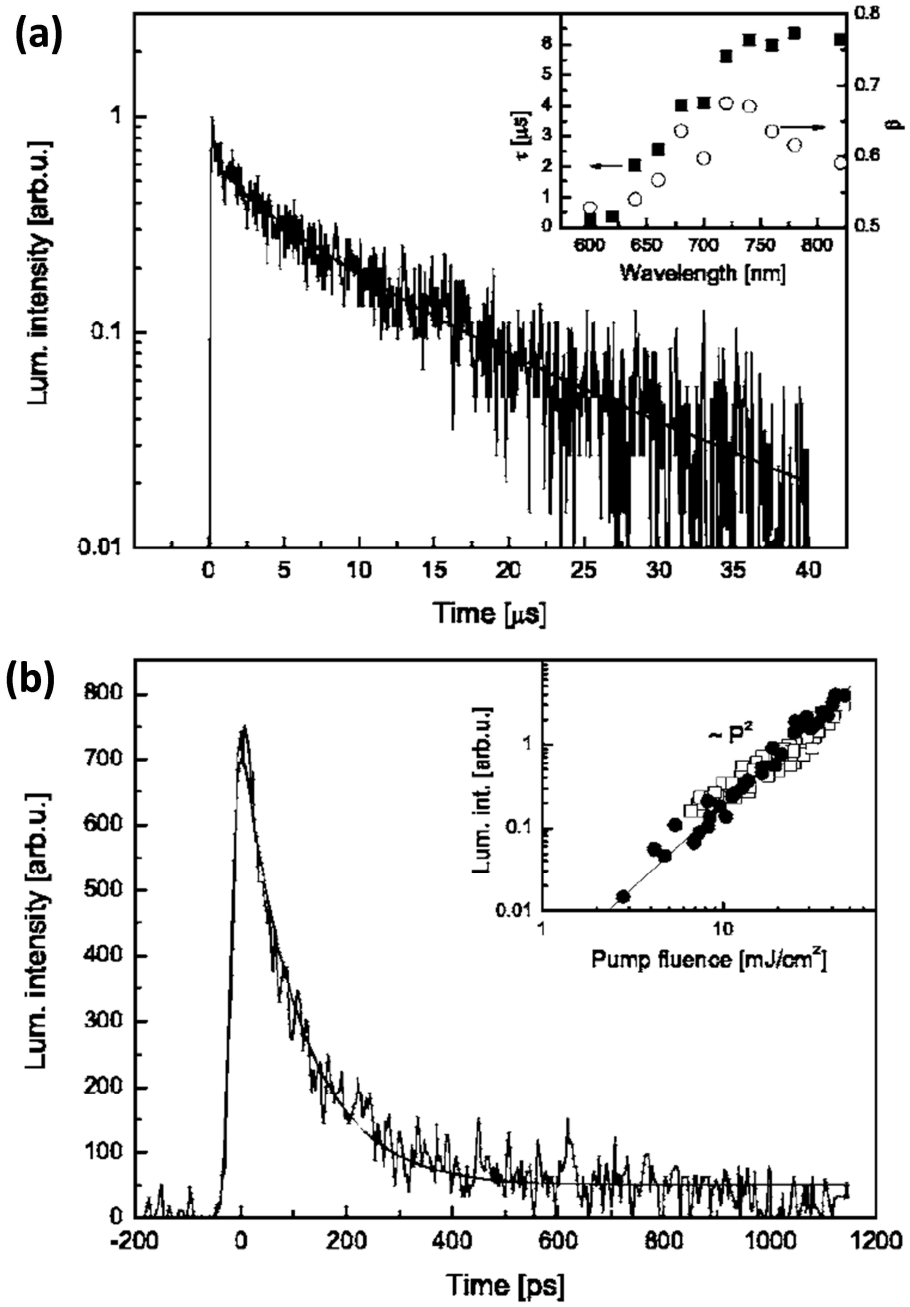

Fig. 9. (a) Microsecond PL decay at 740 nm. Inset: The spectra of parameters $\boldsymbol{\tau}$ and $\boldsymbol{\beta}$. (b) Picosecond PL decay at 600 nm. Inset: Quadratic pump fluence dependence of amplitudes of the fast components (Produced from Ref. [28]).

The fast decay component is shown in Fig. 9(b). It could be fitted by a single exponential decay function with time constant of τ = 105 ps. Meanwhile, the theoretical value of Auger recombination time is given by $\tau_A = \frac{1}{Cn^2}$, where *C* is the Auger coefficient and *n* is the photoexcited electron density. For NCs with two paris of excitons, $n = 2/V$, where V is the NC volume. Condering NCs with diameter of 3 nm and taking $C = 4 \times 10^{-31}$ cm^6s^{-1}, τ_A is found to be 120 ps. This is in very good agreement with observed PL decay time, which confirms that the fast component in PL decay is indeed attributed to Auger recombination of biexcitons.

CHAPTER 5

EXPERIMENTAL STUDIES OF

BURIED JUNCTION SILICON NANOWIRE/NANOWALL SOLAR CELL

In order to explore the novel optical and electrical characteristics of silicon nanostructures, two types of solar cells with different p-n junction structures were fabricated, namely buried junction SiNW solar cell and core-shell SiNW solar cell. In this chapter, the design, fabrication and performance analysis of buried junction device is discussed, which mainly highlights the light trapping property of SiNWs.

5.1 Device design

In the buried junction device, a vertical SiNWire or SiNWall array covers the entire surface of bulk p-type Si (approximately 760 µm thick), to facilitate more efficient light absorption as compared to planar Si absorber. The length of the nanostructure array is approximately 1.3 µm, a reasonable compromise between effective reflectance reduction [37] and technical feasibility with our laboratory facilities (Fig. 10).

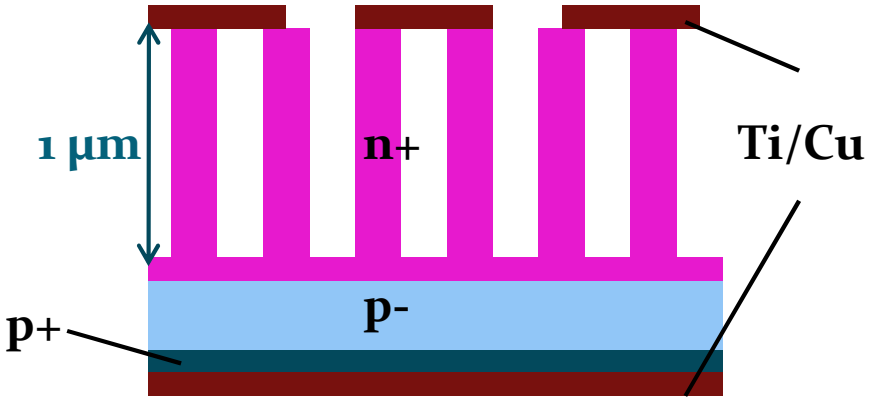

Fig. 10. Cross-sectional schematic diagramme of buried junction SiNWire/SiNWall solar cell.

The p-n junction is located underneath of the nanostructures, such that carrier separation occurs in the bulk region only, and SiNWires/SiNWalls serve only as an absorber. This is to isolate the effect of optical reflectance reduction on the improvement of PCE in our analysis. A back surface field is created by raising the p-type doping on the bottom of the device, in order to minimise carrier recombination at the rear surface.

Ti/Cu metal electrodes are located on top and bottom surface of the cell. Ti serves to provide better adhesion between Cu and Si surface, while Cu ensures high electrical conductance in the metal electrode. While the bottom electrode is a continuous metal layer, the top electrode is in a form of metal grids through which light is allowed to pass through the nanostructures below.

5.2 Fabrication

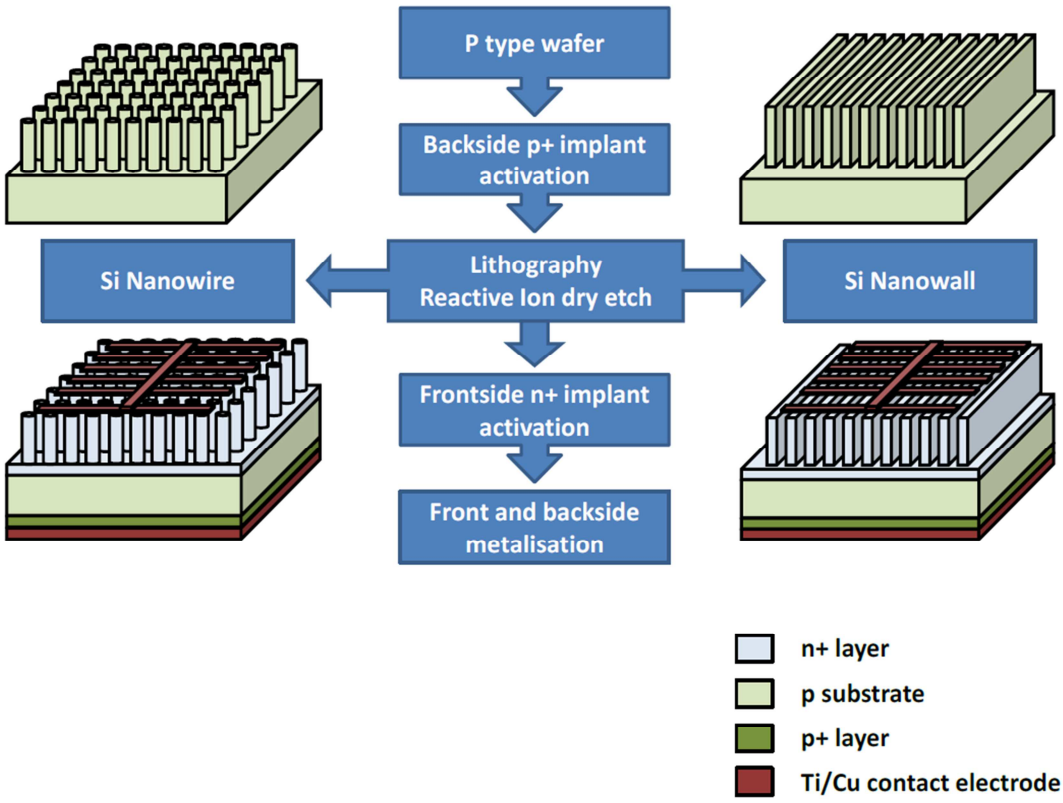

Fig. 11. Process flow schematic of buried junction SiNW (left) and SiNWall (right).

Key steps in the experimental procedure of a SiNWire and SiNWall buried junction cell are illustrated in Fig. 11. The staring material is 8 inch p-type Si(100) wafer with resistivity in the range of 1-50 Ω cm. Back surface field (BSF) [38] is created by BF_2 implant to form a highly doped p+ layer, in order to minimize carrier recombination at rear surface of the cell. The front surface was patterned using standard KrF deep ultraviolet (DUV) lithography followed by resist trimming in O_2 plasma, to form a

matrix of organic resist nano-hemispheres with diameter of 200 nm. The surface was etched in SF_6 based plasma to form arrays of 1.3 µm long SiNWs. Resist was then stripped in O_2 plasma, and the wafer further cleaned in a sulphuric acid-hydrogen peroxide mixture (SPM) to remove any organic residual.

Subsequently, p-n junction was formed by phosphorus implant with energy of 20 keV and dose of 4 x 10^{15} cm^{-2}. A small tilt angle was deployed during the implant to ensure the formation of p-n junction in regions directly below the nanostructures. The dopants were activated by a rapid thermal annealing at 1000 °C for 5 seconds.

A layer of Ti/Cu with thickness of 100 nm/500 nm was sputtered onto the back and top surface of the cell as electrodes. Ti serves to provide better adhesion between Cu and Si surface, while Cu ensures high electrical conductance in the metal electrode. The bottom electrode is a continuous layer of metal film, while the top electrode is in a form of metal grid which allows light to pass through onto the SiNWires underneath. The shading area of the metal grid is approximately 30% of the entire top surface.

For SiNWall device fabrication, the procedure is identical to that of SiNWire device except for long and thin stripes (100 nm thick) of the photoresist being formed on the Si surface during lithography patterning, to define the formation of 2D nanowalls during Si etch step (Fig. 11). Meanwhile, planar control device was created with similar starting wafer and under identical process conditions as fore-mentioned, omitting the plasma etching step for SiNW formation.

Optical reflectance data was obtained using integrating sphere on a Shimazu UV 3600 UV-VIS-NIR Spectrometer. Electrical performance was tested and characterized under a standard AM 1.5G solar simulator.

5.3 Results and discussion

5.3.1 Device formation

The SiNWire and SiNWall devices are both formed by optifccal lithography defined plasma etching. In the arrays of nanostructures etched, excellent uniformity is observed in both SiNWire [Fig. 12(a)] and SiNWall [Fig. 12(b)] device. The length of the nanostructures is approximately 1.3 µm and the width is 100 nm [Fig. 13(a)]. Single-crystallinity is confirmed by high resolution cross-sectional Transmission Electron Microscopy (TEM) imaging [Fig. 13(b)].

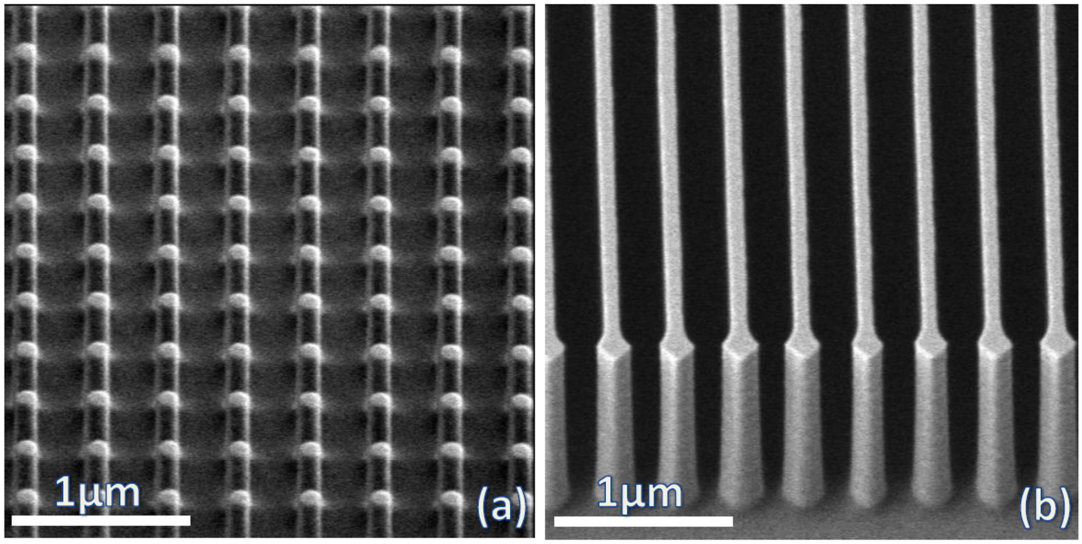

Fig. 12. 45° tilt SEM image of (a) SiNWire array; (b) SiNWall array after plasma etching.

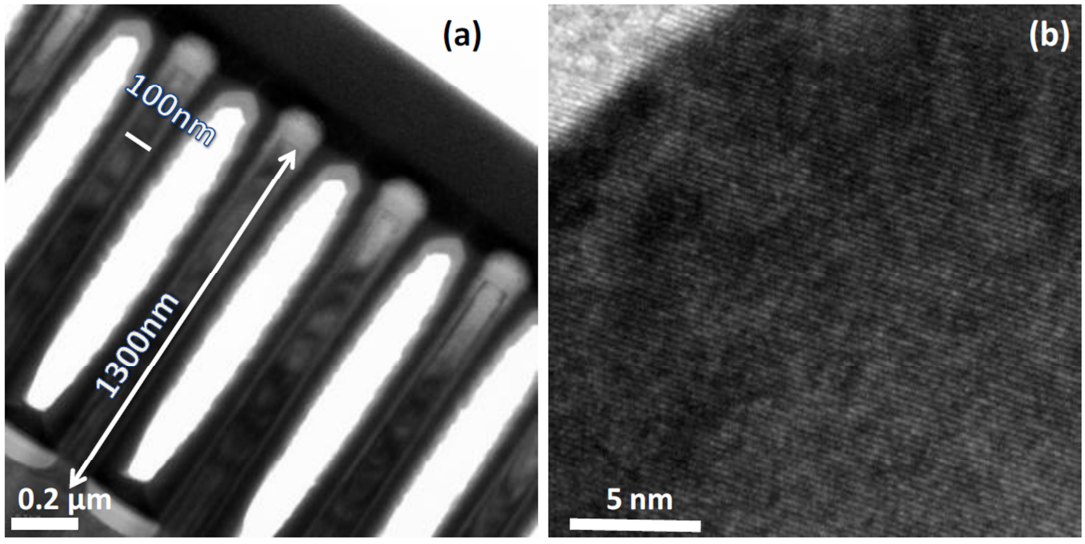

Fig. 13. (a) Cross-sectional TEM of SiNWires; (b) HRTEM image of SiNWire's cross-section.

5.3.2 Optical reflectance measurement

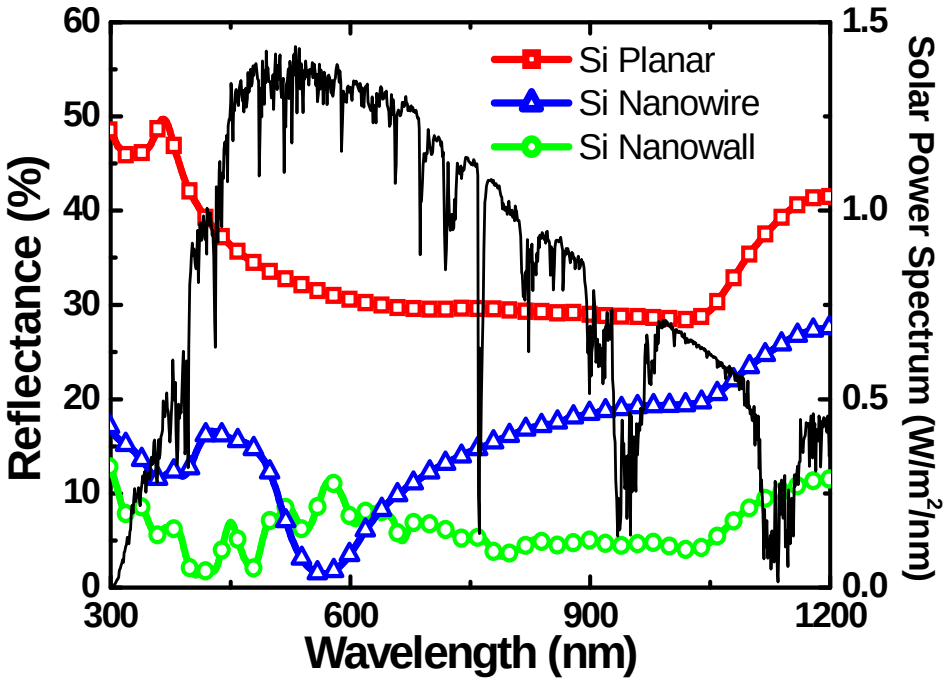

Fig. 14. Optical reflectance of Si planar, SiNWire and SiNWall surfaces versus wavelength. Black curve represents the solar irradiance spectrum at AM 1.5G illumination.

The percentage reflectance values at various wavelengths are plotted in Fig. 14. A comparison between the data for planar Si (red curve) and Si nanostructure covered surfaces (blue and green curves) shows a drastic decrease in reflectance between 300 nm to 1200 nm. The slight discontinuity of the curves observed at around 830 nm is caused by switching of photodetector by the spectrometer at this particular wavelength. Reflectance of planar Si is generally above 30% over the entire range of

wavelengths measured. SiNWire covered surface has a suppressed reflectance of 10-20%, while SiNWalls are able to further reduce the reflectance to <10%.

For a quantitative analysis of the change in total incident power reflected, incident spectral irradiance under AM 1.5G illumination (Fig. 14 black curve) are multiplied by corresponding percentage reflectance values, to obtain the reflected spectral irradiance from 300 nm to 1200 nm. Total percentage of incident irradiance reflected over the entire range of wavelengths is calculated. It is found that planar Si reflects 32% of the total solar irradiance incident on the surface. Significant suppression is observed for nanostructure textured surfaces, with total percentage of solar irradiance reflected being 13.3% and 6.0% for SiNWires and SiNWalls respectively.

SiNWall covered surface demonstrates a larger reduction in total reflectance as compared to SiNWire covered surface. This result is consistent with the different structures of the two devices. It is well received that in diffraction grating-like structures, the zeroth-order transmission is inversely proportional to the pattern's filling ratio [39]. In our work, the filling ratio of SiNWall array is 28.6%, largely surpassing that of SiNWire array (4.9%). Thus we can expect significantly lower zeroth-order transmission though the nanowalls, implying less light reaching the bulk Si surface and reflecting back. As a result, in nanowall arrays, a larger percentage of incident light is diffracted to tilted propagation path where stronger interaction with the nanostructures takes place, leading to enhanced light trapping and reduced reflection.

5.3.3 I-V characterisation

In order to highlight the improvement in performance brought by Si nanostructures, a comparison of electrical characteristics among SiNWire buried junction devices, SiNWall buried junction devices and planar Si control devices was made. Five devices from each of the 3 categories were fabricated and tested under a solar simulator and the average results are summarised in Table 3. The top cell area which was exposed to solar radiation is 1 cm^2, which includes 30% of shading covered by front metal grid.

Table 3. Summary of optical and electrical characterisation of buried junction Si planar, SiNWire and SiNWall solar cell.*

	Si Planar	SiNWire	SiNWall
Reflectance	>30%	10-20%	<10%
Total reflectance of solar irradiance	32.0%	13.3%	6.0%
J_{sc} (mA/cm2)	17.5	23.3	24.9
V_{oc} (mV)	550	560	528
Fill Factor	73.6%	62.8%	47.9%
R_s (Ωcm^2)	1.37	3.10	7.86
PCE	7.1%	8.2%	6.3%
PCE without R_s	7.4%	9.5%	9.8%

* For all three types of cells, top area is 1 cm2, including 30% shading by front metal grid

The increase in light generated current is the main contributor to PCE improvement. SiNWire device attains a short circuit current (J_{sc}) of 23.3 mA/cm^2 while SiNWall

device achieves that of 24.9 mA/cm^2, showing a 33% and a 42% increase respectively, as compared to J_{sc} of planar Si device (17.5 mA/cm^2). The enhancement results from optical properties of the Si nanostructures only as the p-n junction is still buried under the bulk Si surface. This verifies the excellent anti-reflection effect of the Si nanostructures. As expected, SiNWall device is capable of demonstrating 12% more increase in J_{sc} than SiNWire device, as a result of better light trapping and improved absorption by the nanowall structures.

The overall PCEs of planar Si device, SiNWire device and SiNWall device are 7.1%, 8.2% and 6.3% respectively. It should be noted that the PCE obtained for planar Si device is far below the PCE that could be achieved by planar cells with anti-reflection coating (approximately 15%) [48]. This could be attributed to the absence of anti-reflection coating on the planar Si control devices in this work.

SiNWire device shows only 15.5% increase of PCE as compared to planar device, while SiNWall device has lower PCE than that of Si planar device. Despite the drastic improvement in light absorption and J_{sc}, overall efficiencies of Si nanostructure based solar cells are compromised mainly because of low fill factors. The fill factor of SiNWire and SiNWall device are 62.8% and 47.9% respectively, accounting for the adverse effect on their efficiencies.

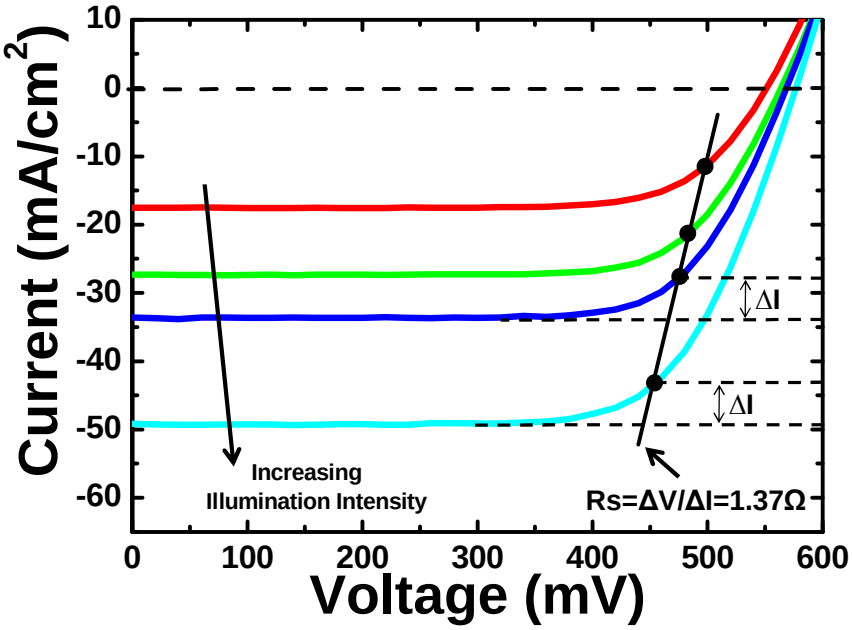

Fig. 15. Series resistance measurement of buried junction Si planar solar cell, demonstrating multiple illumination intensity method [40].

In order to quantify the effect of series resistance R_s on device performance, multiple illumination intensity method [40] is employed to evaluate R_s for all three types of solar cells, as demonstrated in Fig. 15 for the case of Si planar device. I-V data are obtained under four different illumination intensities. For every I-V curve, a constant arbitrary small change in light-generated current ΔIL is defined, to located the data point in the fourth quadrant such that $|I| = I_{sc} - \Delta IL$ (Fig. 15) These four points obtained are fitted with a linear regression line, which has a slope of $1/R_s$. R_s of SiNWire device is extracted to be 3.10 Ω, about 2 times larger than that of planar Si control device (1.37 Ω, see Fig. 15). SiNWall device is found to have a significantly higher R_s of 7.86 Ω, nearly 6 times higher than that of planar Si device. This result is

consistent with the difference in surface topology among the three devices. The deposited metal layer is thinner on the sidewalls of high-aspect-ratio nanostructures than that on planar surfaces, resulting in higher resistance in the top metal electrode for SiNW device. The long and narrow geometry of the nanostructures therefore contributes to larger resistance. The relatively large R_s found the nanowall samples could be attributed to poor gap filling ability of the metal sputtering technique (*See Chapter 6, Section 6.3*), since in nanowall structure the requirement for the metal conformal deposition is more stringent than wires. This issue can be solved by the adoption of more conformal metallization method such as electroplating or atomic layer deposition.

The high value of R_s in our devices is due to non-optimized metallization process and can readily be lowered to a typical value of ~ 0.1 Ωcm^2 [41], upon process optimization. The intrinsic PCE of the devices are estimated to be 9.5% and 9.8% for nanowire and nanowall devices respectively (Table 3).

CHAPTER 6

EXPERIMENTAL STUDIES OF

CORE-SHELL SILICON NANOWIRE SOLAR CELL

In addition to excellent anti-reflection property of nanostructures which greatly enhances silicon solar cell performance, carrier collection efficiency could be further improved by orthorgonalisation of carrier generation and transport by incorporating core-shell nanowire structure in the device design. The principle of performance enhancement by core-shell junction is discussed in Chapter 3. In this chapter, we focus on the design, fabrication and characterisation of core-shell SiNW solar cell, in order to explore and investigate the advantages of radial p-n junction in PV applications.

6.1 Device and process design

6.1.1 Device structure

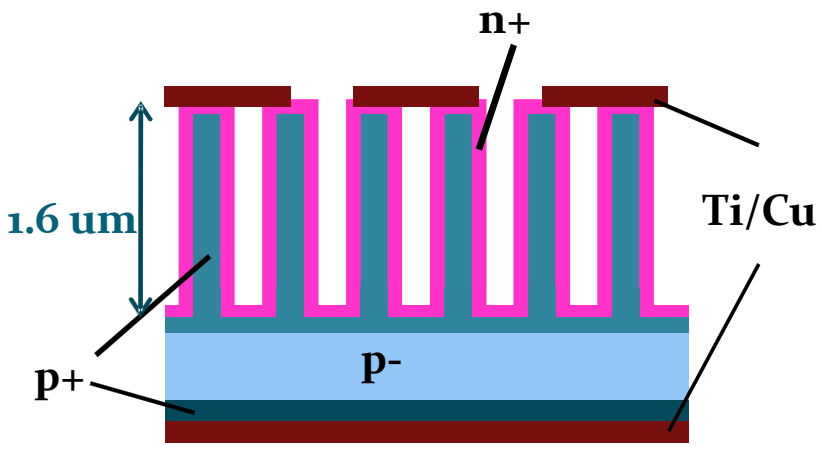

Fig. 16. Cross-sectional schematic diagramme of core-shell SiNW solar cell.

The physical structure of core-shell SiNW device is similar to that of buried-junction device discussed in Chapter 5, including the back surface filed and metal electrodes. However, instead of being buried under the bulk Si surface, p-n junction is now located in the radial direction of each nanowires (Fig. 16), which consists of a p type core and n type shell. This enables the electron-hole pairs to be generated near the surface of nanowires and creates a shorter distance for carrier transport. The average diameter of nanowires is 200 nm and the length is approximately 1.6 μm, which facilitates light absorption in the axial direction and carrier transport in the radial direction.

6.1.2 *P-n junction profile simulation*

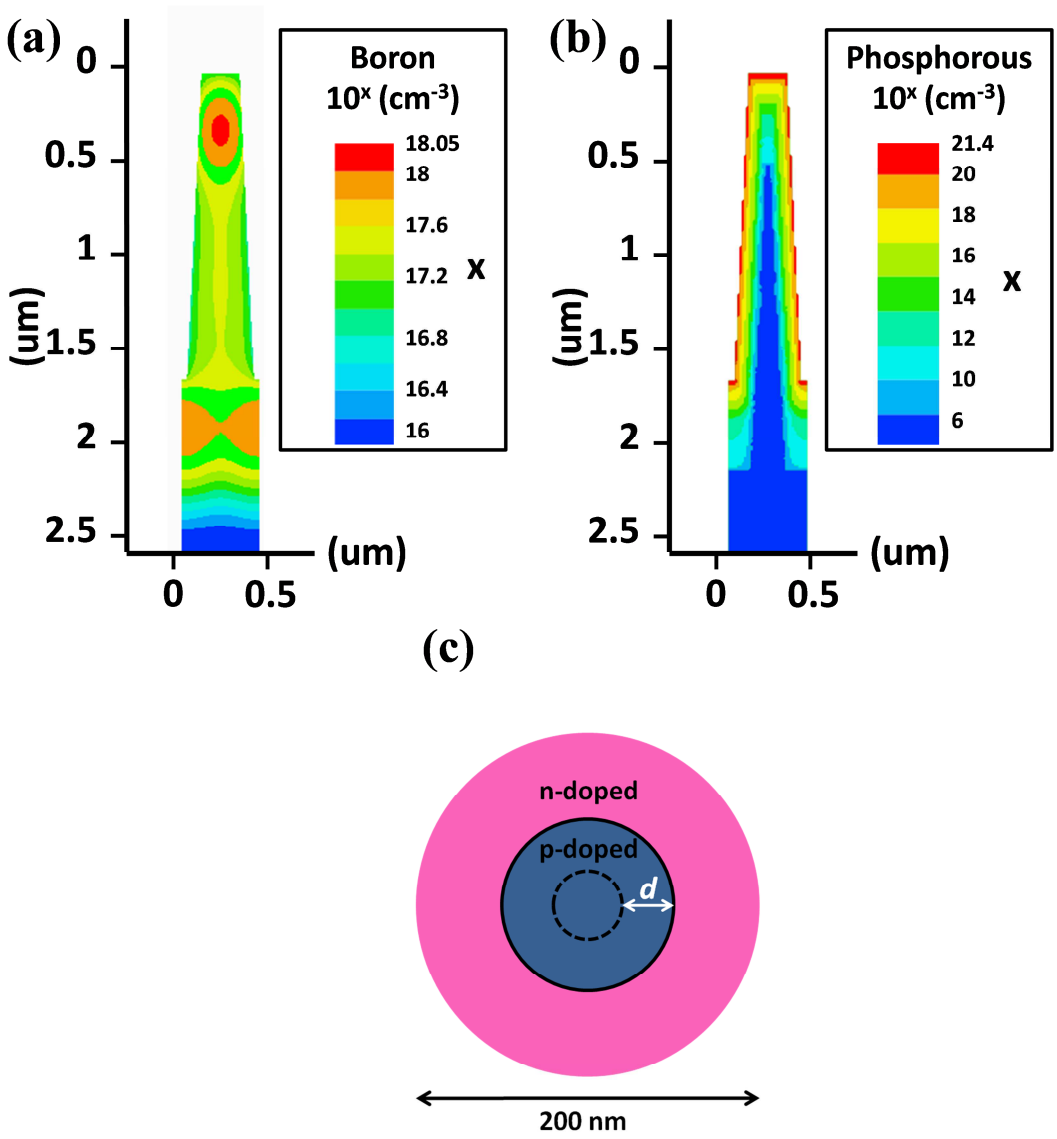

Fig. 17. (a) Simulated boron profile in a nanowire after BF_2 core implant (rotation: 0°, 90°, 180°, 270°; dose: 2.5 x 10^{13} cm^{-2}, energy: 80 keV, tilt: 7° for each rotation) and 1 hour drive-in at 1000 °C. (b) Simulated phosphorus profile in a nanowire after P shell implant (rotation: 0°, 90°, 180°, 270°; dose: 10^{15} cm^{-2}, energy: 7 keV, tilt: 7° for each rotation). The color gradient depicts distribution of different dopant concentrations in the vertical cross-section of the wire. Junction depth (at which both dopant concentrations are

approximately equal) is estimated to be 50 nm. (c) A schematic illustration of the radial p-n junction in a nanowire, indicating the estimated junction depth and depletion width *d*.

To form a continuous and uniform n type shell around the relatively thin nanowires requires doping methods with sufficient controllability. As high resistance in depletion region is undesirable for collection of light generated carriers [42], it has been remarked that depletion width in the nanowires must be kept small [9]. This requires the formation of a highly doped p-n junction. Because of insufficient doping in the starting wafer (~10^{16} cm^{-3}), a core doping step is essential to increase boron concentration, so as to reduce the depletion width and to ensure a un-depleted core needed for transport of holes. A four-rotational ion implant is used for both core and shell doping, with conditions (implant dose, energy and tilt angle) pre-determined by numerical simulation using T-SUPREM4. The result of simulation demonstrates that after the core implant and drive-in, boron concentration has been increased to approximately 7 x 10^{17} cm^{-3} in the core of the nanowires [Fig. 17(a)]. The subsequent shell implant forms a thin and uniform n+ sheath, with a phosphorus concentration of around 10^{21} cm^{-3} on the wire surface [Fig. 17(b)]. The p-n interface is located at around 50 nm under the nanowire outer surface, where both boron and phosphorus concentrations are approximately equal. Assuming non-degeneracy in Si, built-in voltage of the p-n junction is estimated to be 1.06 V according to Eq. (6) [42]:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{{n_i}^2}\right), \qquad \text{(Eq. 6)}$$

where N_D (phosphorus concentration) and N_A (boron concentration) being the dopant concentrations at the junction edges, are 10^{20} cm^{-3} and 7 x 10^{17} cm^{-3} respectively. *k* is

the Boltzmann constant, and T is temperature which is taken to be 300 K in this work. n_i is the intrinsic carrier concentration in Si at 300 K. Deriving from Gauss's Law, an estimation of total depletion width is given by Eq. (7) [42]:

$$\boldsymbol{d = \sqrt{\frac{2\varepsilon}{q}\frac{N_A+N_D}{N_A N_D}(V_{bi}-V)}}\,, \qquad \text{(Eq. 7)}$$

where ε is the permittivity in Si. d is found to be 44 nm in the absence of external field V, and decreases in the operating regime of solar cell where forward bias is applied (V > 0). Despite the fact that depletion region is located mostly in the p-doped core as a result of N_D being dominantly larger than N_A, the nanowire is not fully depleted [Fig. 17(c)]. If boron concentration were to remain at its initial value (~10^{16} cm^{-3}), depletion width would increase to around 350 nm based on Eq. (6) and (7), leaving the entire wire depleted, thus highlighting the necessity of BF_2 core implant.

6.2 Fabrication

Key steps in the experimental procedure are illustrated in Fig. 18. The starting substrate used was also 8 inch p-type Si(100) wafer with initial resistivity of 1-50 Ω cm. Similar to that in buried junction device, formation of back surface field (BSF) is also required in core-shell SiNW device (See Chapter 5 Section 5.2). Organic resist was deposited onto to top surface by KrF deep ultraviolet (DUV) lithography patterning, followed by trimming in O_2 plasma to form a regular array of nano-hemispheres of 200 nm in diameter, thus defining the critical dimension of the nanowires to be etched.

SiNWs of 1.6 µm in lengths were etched from the patterned Si surface, in a SF_6 based plasma. The etching process is followed by resist stripping in O_2 plasma and rinse in SPM to remove organic residual.

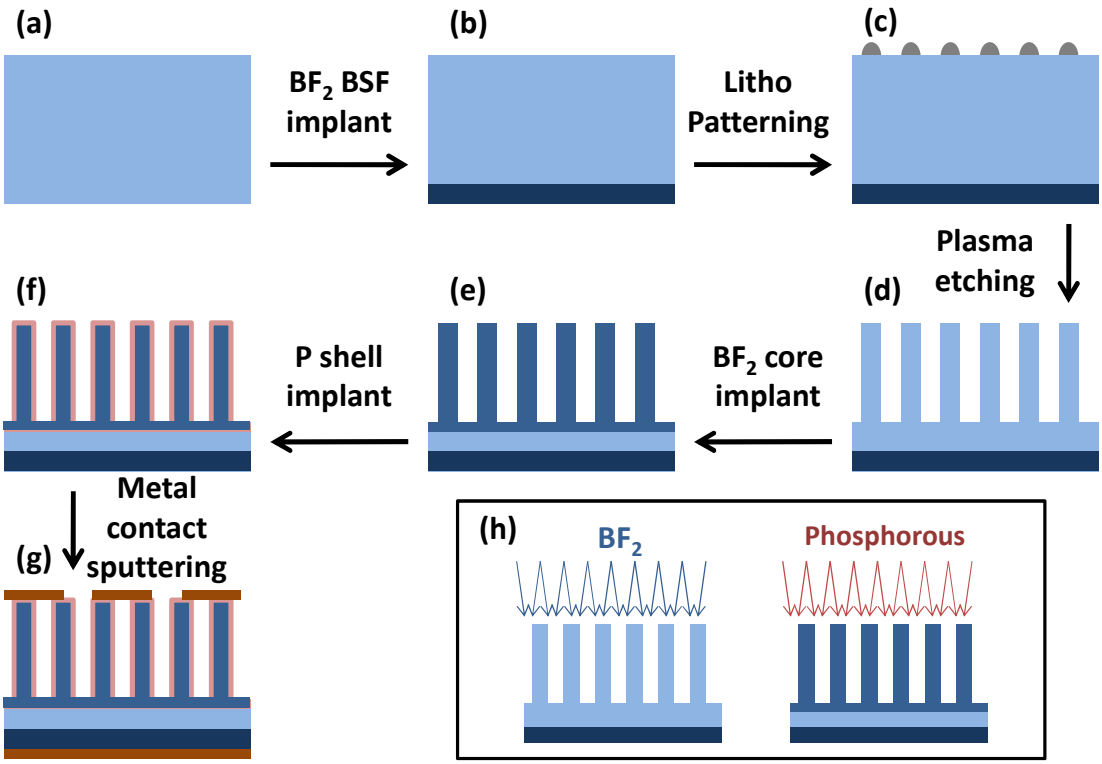

Fig. 18. Schematic demonstration of fabrication process of core-shell SiNW solar cell. (a) Starting p-type Si test wafer. (b) BSF formation by BF_2 implant. (c) DUV lithography patterning and resist trimming. (d) SiNW fabrication by SF_6 based plasma etching. (e) BF_2 implant to increase core dopant concentration. (f) Phosphorus shell implant. (g) Metal contact formation. (h) Illustration of four-rotational ion implantations for BF_2 core implant (Left) and phosphorus shell implant (Right). Each stage consists of four sub ion implant steps, with rotation of 0°, 90°, 180° and 270° respectively and a vertical tilt of 7° for every implant. BF_2 core implant was done with dose of 2.5 x 10^{13} cm^{-2} and energy of 80 keV; phosphorus shell implant was done with dose of 10^{15} cm^{-2} and energy of 7 keV.

Two separate ion implantation processes were used for core and shell formation respectively [Fig. 18(h)]. The as-etched SiNW arrays first underwent a four-rotational BF2 implant with a dose of 2.5 x 10^{13} cm^{-2}, energy of 80 keV and a vertical tilt angle of 7° for each rotation. The drive-in process was a furnace annealing at 1000 °C for 1 hour, to yield a more uniform distribution of p-type dopant in the wires. Subsequently, a similar four-rotational phosphorus implant was carried out with a dose of 10^{15} cm^{-2} and energy of 7 keV, followed by a 5 second rapid thermal annealing process at 1000 °C to convert the outer shell of the wires to n-type. The implant and annealing conditions were carefully tailored by simulation (T-SUPREM4) to ensure the formation of a uniform and shallow radial junction (See Section 6.1.2).

A continuous film of Ti/Cu with thickness of 100 nm/500 nm was sputtered onto the back surface of the cell as bottom electrode. Ti serves to provide better adhesion between Cu and Si surface, while Cu ensures high electrical conductance in the metal electrode. A similar Ti/Cu layer was then sputtered through a shadow mask to form metal grids on the front surface, thus completing the fabrication process of the SiNW based solar cell. Meanwhile, planar control device was created with similar starting wafer and under identical process conditions as fore-mentioned, omitting the plasma etching step for SiNW formation. Similar to that of buried junction and Si planar control devices, top cell area is 1 cm^2, 30% of which covered by metal grid.

To facilitate I-V measurement, back surface of the device was fixed to a conductive substrate by silver paste, and a conductive rod was attached to front side metal grid as extended top electrode [Fig. 19(e)]. Optical reflectance data was obtained using integrating sphere on a Shimazu UV 3600 UV-VIS-NIR Spectrometer. Electrical performance was tested and characterized under a standard AM 1.5G solar simulator.

6.3 Results and discussion

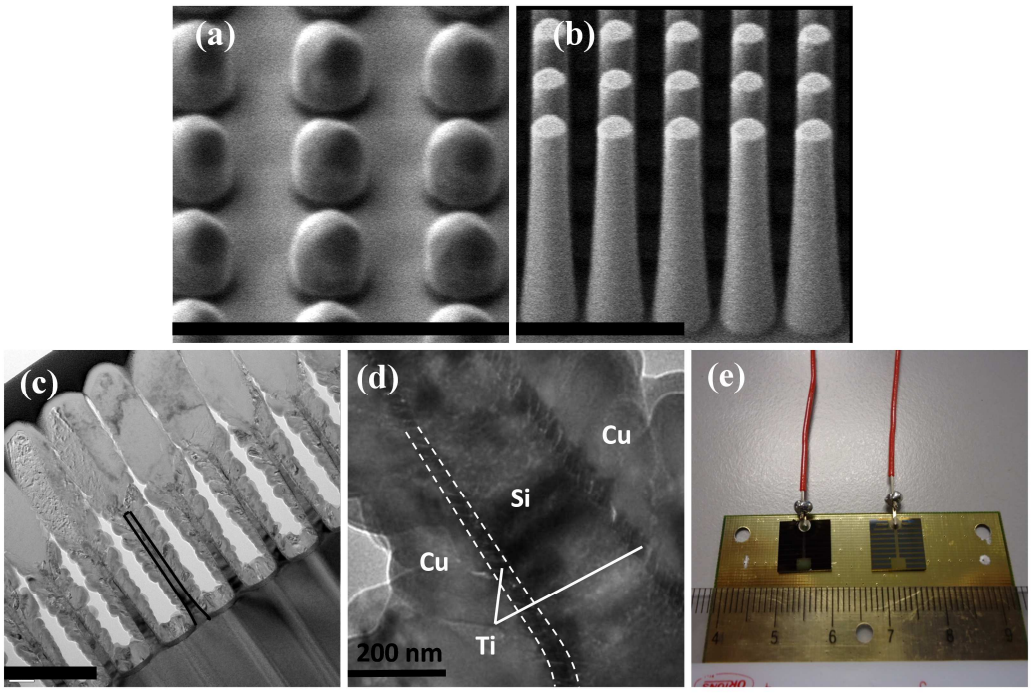

Fig. 19. (a) 45° tilt Scanning Electron Microscope (SEM) image of resist nano-hemispheres on Si surface after lithography patterning and resist trimming. (b) 45° tilt SEM image of SiNW array formed by plasma etch. (c) Transmission Electron Microscope (TEM) image of SiNW device cross-section near the top surface where metal grid is deposited. The dark outline indicates the border of a nanowire under the grayish metal layer. (d) Enlarged view at the metal-Si interface of a nanowire. (e) 45° tilted top view of complete SiNW device (left) and planar Si control device (right) under visible light. Dark scale bars in (a)-(c) represent 1 μm.

Fig. 19 shows the SiNW device at various stages of fabrication. After DUV lithography patterning, a matrix of nano-hemispheres is formed on the top surface of Si wafer [Fig. 19(a)]. Such excellent uniformity and periodicity persists in the SiNWs etched, which are approximately 1.6 μm long and 200 nm in diameter [Fig. 19(b)]. They are observed to have a smooth outer surface, without any visible rough patch or surface defect. The vertical SiNWs with inter-wire spacing of 200 nm take up approximately 30% of the entire array volume. Near the front surface where top electrode is deposited, voids are seen between nanowires beneath the metal layer [Fig. 19(c)], which could be attributed to the limited gap-filling ability of the sputtering process. Nonetheless, Ti adheres to SiNW surface in a rather conformal manner [Fig. 19(d)], assuring an effective barrier between Cu and Si to avoid possible degradation of carrier lifetime caused by Cu diffusion. The metal grid covers approximately 30% of the entire 1 x 1 cm^2 top surface [Fig. 19(e)].

6.3.1 Optical reflectance measurement

SiNW device displays a darker surface under visible light as compared to planar control device [Fig. 19(d)], indicating less optical reflection on the top surface of the device. This observation is confirmed by reflectance measurement using integrating sphere. The percentage reflectance values at various wavelengths are plotted in Fig. 20(a). A comparison between the data for planar Si and SiNW surface shows a drastic decrease in reflectance between 300 nm to 1200 nm. The slight discontinuity of the curves observed at around 830 nm is caused by switching of photodetector by the spectrometer at this particular wavelength. Reflectance of planar Si is generally above 30% over the entire range of wavelengths measured, while reflectance of SiNW surface is suppressed to less than 12%.

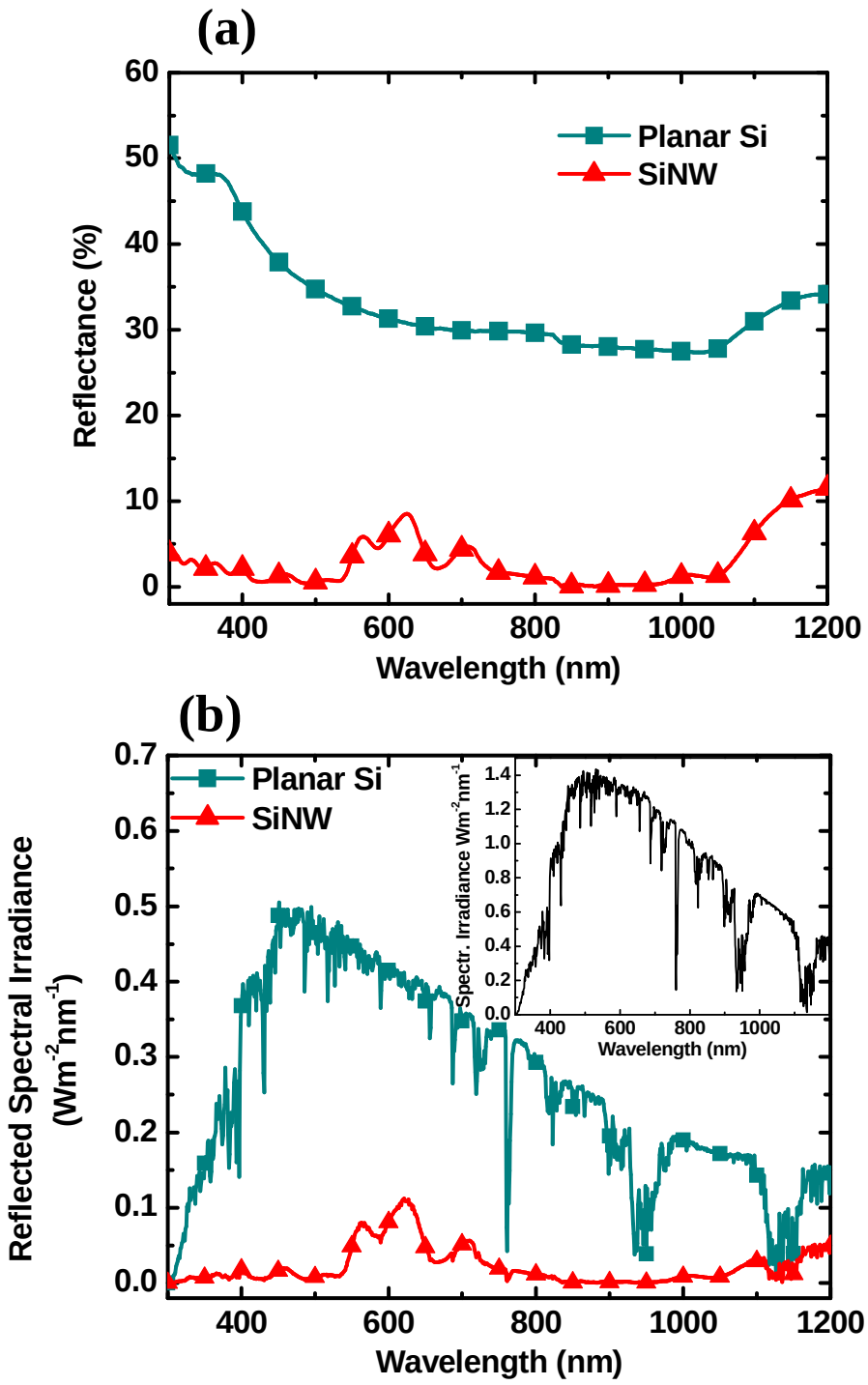

Fig. 20. (a) Reflectance data of SiNW surface and planar Si surface, measured using integrating sphere. (b) Reflected spectral irradiance of SiNW surface comparing with that of planar Si surface; the inset shows incident spectral irradiance under standard AM 1.5G illumination. The measurements were taken without the front metal grid on cell surface.

For a quantitative analysis of the change in total incident power reflected, incident spectral irradiance under AM 1.5G illumination [Fig. 20(b) inset] are multiplied by corresponding percentage reflectance values, to obtained the reflected spectral irradiance from 300nm to 1200 nm [Fig. 20(b)]. Total percentage of incident irradiance reflected over the entire range of wavelengths is calculated. It is found that planar Si surface reflects 32% of the total incident irradiance, while SiNW surface reflects only 2.7%, a 92% suppression as compared to planar surface. The sub-wavelength diameter of the wires is responsible for more effective light scattering and light trapping [13,37,43]. Thus even with a moderate filling ratio of 30% and a length of only 1.6 µm, the SiNW array is able to reduce total reflection of incident solar irradiance to only 8% of that reflected by planar Si surface.

6.3.2 I-V characterisation

Table 4. I-V characterisation of planar Si and core-shell SiNW solar cell.

	Planar Si	Core-shell SiNW
J_{sc} (mA/cm^2)	9.34	14.2
V_{oc} (V)	0.548	0.485
FF	72.8%	42.9%
R_s (Ω)	0.95	12.9
PCE	3.7%	3.0%
FF[a]	74.0%	63.9%
PCE [a]	3.8%	4.4%
J_{sc} [b] (mA/cm^2)	13.3	20.3
PCE[b]	5.3%	4.2%
PCE[a,b]	5.4%	6.3%

[a]In the absence of R_s.

[b]In the absence of 30% shading losses.

Five core-shell SiNW based devices and five Si planar control devices were fabricated. Their electrical characteristics tested under a solar simulator, and the average results summarised in Table 4. As the devices have top area of 1 x 1 cm^2, the currents measured are equivalent to the values of current density. From the I-V curve of SiNW device under dark and AM 1.5G illumination [Fig. 21(a)], a clear rectifying behaviour is observed. An expanded I-V plot in forward bias [Fig. 21(b)] shows that SiNW device has an open circuit voltage (V_{oc}) of 0.485 V, a short circuit current density (J_{sc}) of 14.2 mA/cm^2 and a fill factor (FF) of 42.9%. The PCE is calculated to be 2.95%, which is significantly higher than that of previously reported SiNW based solar cells with radial p-n junction [16-18,20,21,37]. J_{sc} and V_{oc} of the planar Si control device are found to be 0.548 V and 9.34 mA/cm^2 respectively. The 52% increase of J_{sc} in SiNW based device is attributed to improved light absorption in SiNW arrays and increased junction area from the radial p-n junction. However, it should be remarked that identical four-rotational ion implantation processes are used for junction formation in both SiNW and planar Si device. For SiNW device, each of the four implants is responsible for doping a vertical nanowire from a different angle, thus the dopant ions are not all incident onto the same plane. While for planar Si device, the top surface receives all incident dopant ions in four implants, thus forming a p-n junction with possibly higher dopant concentration and more severe substrate damage. The low J_{sc} in planar device could be partially attributed to recombioation caused by ion implantation-induced defects. As a result, the PCE in planar device in this section is relatively poor as compared to that fabricated with the buried junction SiNW devices (*See Chapter 5 Section 5.3*). In addition, the absence of anti-reflection coating could have resulted in the PCE of planar control device in this section being far below the typical PCE of other laboratory solar cells [48].

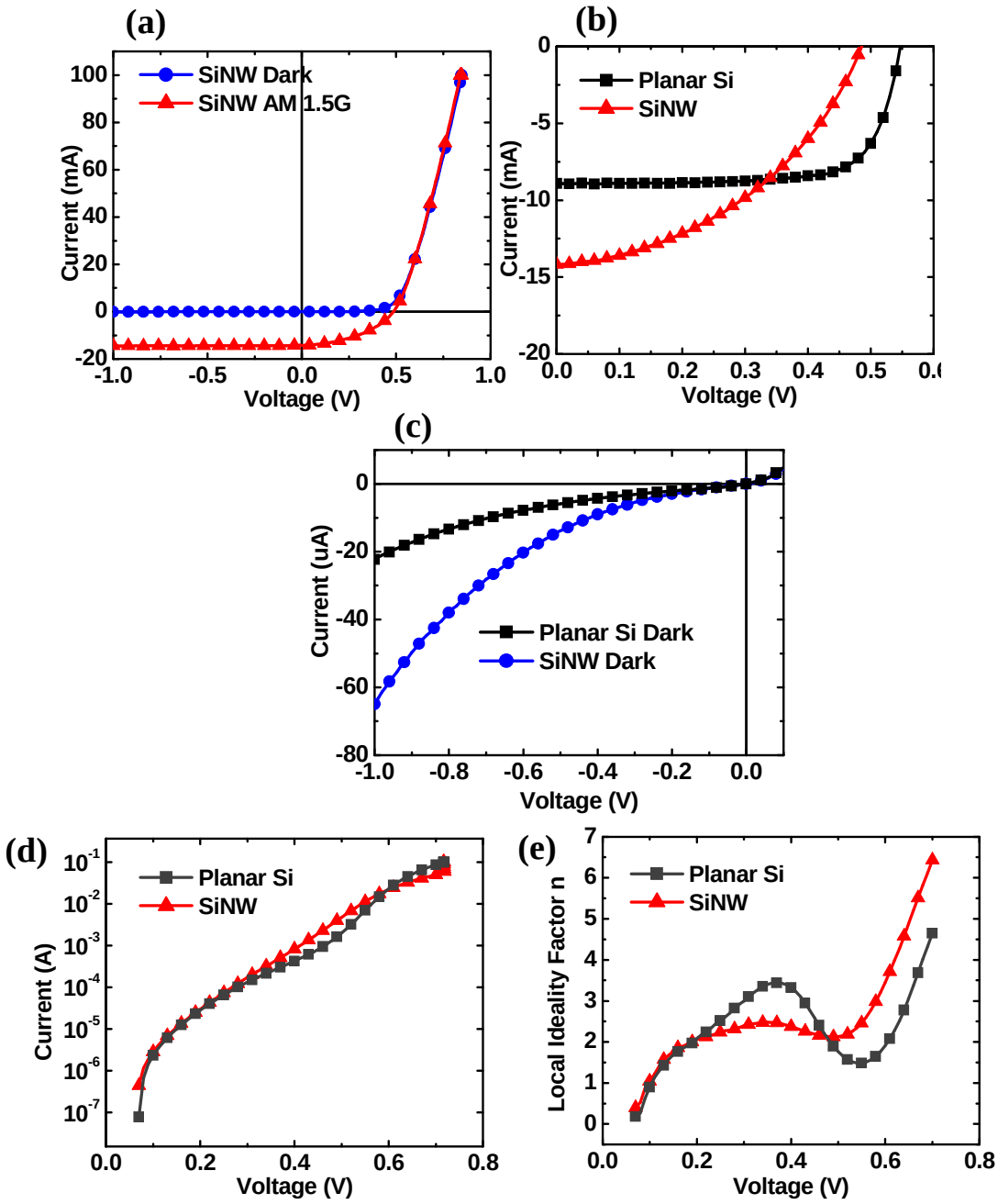

Fig. 21. (a) I-V characteristic of core-shell SiNW solar cell in dark and AM 1.5G illumination. (b) Comparison of I-V characteristic between core-shell SiNW and planar Si solar cell under AM 1.5G illumination. (c) Comparison of dark I-V characteristics between core-shell SiNW and planar Si solar cell in reverse bias region. (d) Semi-log plot of dark current in forward bias region. (e) Local ideality factor as a function of voltage in forward bias region.

A closer analysis of the dark I-V characteristic in reverse bias region [Fig. 21(c)] gives a leakage current of 65 uA at -1 V for SiNW based devices, as opposed to that of 21 uA for planar Si device. Sign of early reverse breakdown is observed for both devices, as a result of a large number of recombination centres caused by high doping at p-n junction [37,42]. Larger leakage current in SiNW based device indicates more recombination as compared to planar Si device, despite the latter having possibly more ion implantation-induced defects near the junction in planar Si device. This observation could be explained by the drastic increase of surface/junction area in SiNW arrays, which creates significantly more recombination sites and results in a higher overall recombination current in SiNW device. By plotting forward bias dark I-V data in a semi-log scale [Fig. 21(d)], local ideality factor *n* could be extracted from the slope. A plot of *n* in forward bias region is shown in Fig. 21(e). For SiNW based device, *n* is 2-2.5 between 0.3 to 0.55 V. There are possibly recombination losses via defects in bulk Si, on nanowire surfaces, at the radial p-n junctions and in the depletion region. Planar Si control device has an ideality factor of 1.5 at around at 0.55 V, confirming less overall recombination. The large peak of *n* for planar Si device is under the effect of shunt resistance arising from the fabrication process, rather than the design and structure of the cell. The major increase in *n* of SiNW device after 0.6 V could be under the impact of series resistance [44].

In order to quantify the effect of series resistance R_s on device performance, multiple illumination intensity method [40] is employed to evaluate R_s for both SiNW and Si planar solar cells, as demonstrated in Fig. 22. I-V data are obtained under four different illumination intensities. For every I-V curve, a constant arbitrary small

change in light-generated current ΔI_L is defined, to located the data point in the fourth quadrant such that $|I| = I_{sc} - \Delta I_L$ [Fig. 22(a)]. These four points obtained are fitted with a linear regression line, which has a slope of $1/R_s$. R_s of SiNW based device is extracted to be 12.9 Ω [Fig. 22(a)], nearly 14 times larger than that of planar Si control device [Fig. 22(b)]. This result is consistent with the difference in surface topology between the two devices. The deposited metal layer is thinner on the sidewalls of high-aspect-ratio nanowires than that on planar surfaces [Fig. 19(c)], resulting in higher resistance in the top metal electrode for SiNW device. Meanwhile, for regions without direct contact to top metal grid, carriers generated in the radial junctions need to travel down the nanowires before being transported to respective electrodes. The long and narrow geometry of the wires therefore contributes to larger resistance.

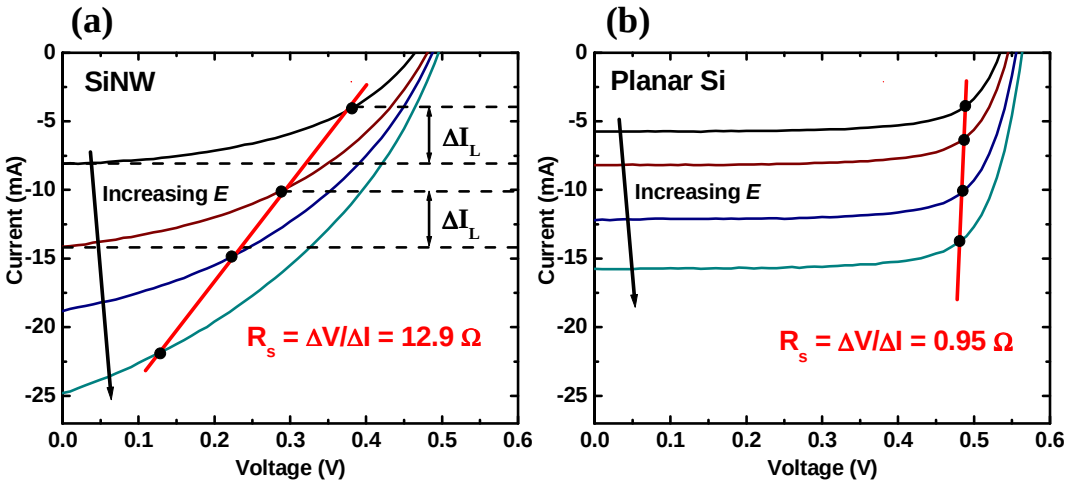

Fig. 22. Evaluation of series resistance using multiple intensity method in (a) core-shell SiNW solar cell and (b) planar Si solar cell. E represents incident illumination on the surface of the device.

The relatively high overall efficiency obtained in this core-shell SiNW based solar cell is mainly contributed by light generated current, which indicates an efficient carrier generation-collection process achievable through this design, even with relatively large resistivity in the starting wafer. To compensate for the short carrier diffusion length associated with defects in the starting wafer, a short collection path is created by using nanowires with small radius (~100 nm). Meanwhile, the four-rotational ion implantation process enables formation of a shallow and highly-doped radial p-n junction, keeping the depletion region small. High carrier mobility near the junction coupled with short collection length effectively reduces loss in J_{sc} caused by recombination.

To further improve the device performance, series resistance needs to be reduced as it is the main cause for low FF. I-V curve of the solar cell under the impact of R_s is given by [45]:

$$\boldsymbol{I = I_0 \exp\left[\frac{q(V_{junction}+IR_s)}{nkT}\right] - I_L}\,, \qquad \text{(Eq. 8)}$$

where I_0 and I_L are dark saturation current and light generated current respectively. $V_{junction} + IR_s$ which equals the terminal voltage measured in the circuit (V), is the sum of voltage drop across the p-n junction of the cell ($V_{junction}$) and voltage drop in series resistance (IR_s). $V_{junction}$ is then obtained such that:

$$\boldsymbol{V_{junction} = V - IR_s}\,, \qquad \text{(Eq. 9)}$$

where V is the voltage obtained in the original I-V data. The "intrinsic" I-V curves with V replaced by $V_{junction}$ are plotted in Fig. 23. Upon eliminating the effect of R_s, FF of SiNW device could improve from 42.9% to 63.9%. This potential improvement observed is significantly lesser in planar control device, as a result of its having a

much smaller R_s. Also, an empirical expression of FF in the absence of parasitic resistances was proposed by M. A. Green [47], that calculates FF directly from V_{oc} and ideality factor n of the device. These two methods yield similar estimated values of "intrinsic" FF.

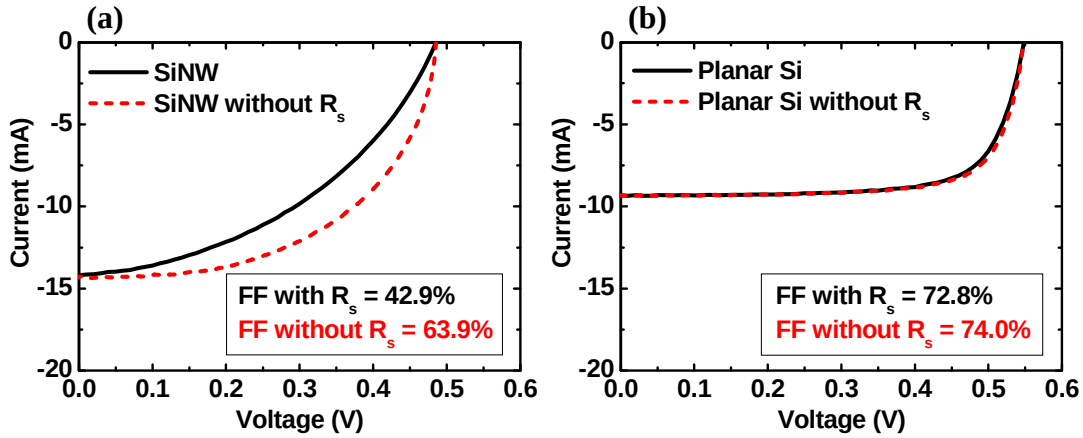

Fig. 23. I-V curves before and after eliminating the effect of R_s for (a) core-shell SiNW solar cell and (b) planar Si solar cell.

FF and PCE without the effect of R_s are also presented in Table 4. It is shown that although PCE of SiNW device fabricated suffered from low FF, it could increase to 4.40% upon eliminating R_s, surpassing the efficiency of planar device. Lower series resistance and higher FF could be achieved by improving experimental techniques. Recent research has demonstrated that a complete filling of metal between nanowires on the top surface helps to achieve FF as high as 60.7% [44]. Deposition techniques such as electroplating would be useful to improve the gap filling of metal in this work.

Meanwhile, there is limitation in junction formation by ion implantation. An inter-wire spacing of 200 nm is sufficient for incident ions with 7° tilt to reach the bottom of 1.6 µm nanowires, if the wire diameter remains constant throughout the entire length. However, because of the tapered structure of our SiNWs [Fig. 19(b)], surface dopant concentration in the part of the nanowires below 1.25 µm might be less than that in the simulated dopant profile (Fig. 17), under the shadowing effect from neighbouring nanowires during ion implantation. This issue could be solved by adopting a more conformal doping method such as plasma doping.

In addition, 30% of the top surface is currently covered by a 600 nm thick metal layer, which effectively prevents incident light from reaching the wires below. If the design of metal grid is optimized to minimize these shading losses, a larger J_{sc} of 20.3 mA/cm^2 and a PCE of 4.21% could be attained for SiNW device. Combining with the elimination of series resistance, PCE could further increase to 6.29% (Table 4). Furthermore, as optical reflectance continues to decrease with nanowires lengths above 2 µm [38], it is possible to further improve light absorption and overall device performance if longer wires are fabricated.

CHAPTER 7

EXPERIMENTAL STUDIES OF

ULTRA-THIN SILICON NANOWIRES FOR MEG APPLICATION

Although multiple-exciton generation (MEG) effect has been observed and confirmed in 0D Si nanocrystals/quantum dots [4], it is yet to be explored in 1D nanowires. As MEG allows the power conversion efficiency (PCE) of a solar cell to surpass the Shockley-Queisser limit of 33.7% [7] to reach a theoretical maximum PCE of 41.9% [12], it has a huge potential in further enhancing the solar cell performance if being incorporated into the SiNW device.

As MEG is significant only in quantum confinement regions [4], one of the most important technical issues in SiNW fabrication for MEG test is to reduce the NW diameters to sub 10 nm. The sharpening mechanism adopted in this project is thermal oxidation, which has been previously utilised to produce ultra-thin silicon nanotips (SiNTs) [32,33].

7.1 Fabrication procedure

SiNW arrays with inter-wire spacing of 400 nm and two different lengths (1 µm and 500 nm) were produced from p-type test wafers by plasma etching to yield initial NW diameters of approximately 90 nm (Fig. 24). The diameters were then reduced by furnace dry oxidation at 975 °C for 3.5 hours.

For the purpose of inspection, some samples had the oxide layer removed by a buffered oxide etch (BOE) and were inspected by a Scanning Electron Microscope

(SEM). NW diameter after this oxidation was approximately 45 nm (Fig. 25), which was substantially larger than the dimensions of quantum confinement (sub 10 nm).

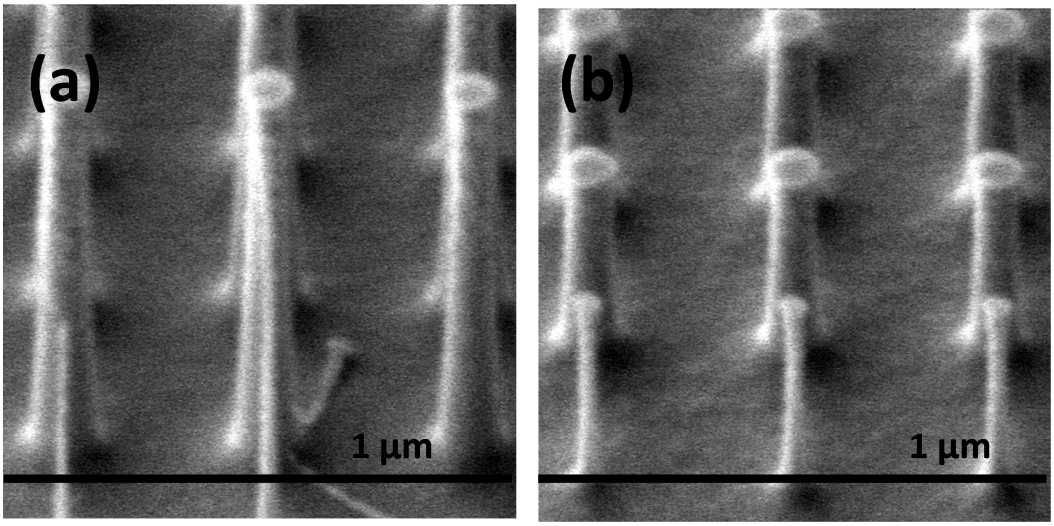

Fig. 24. SEM image of SiNWs with lengths of (a) 1 µm and (b) 500 nm after plasma etching. The diameters are approximately 90 nm.

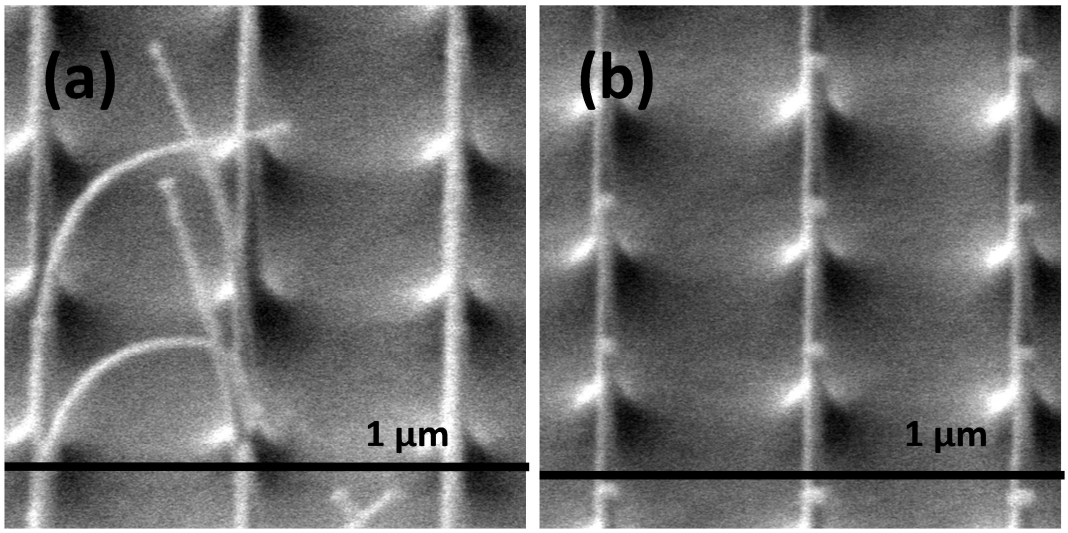

Fig. 25. SEM image of (a) 1 µm and (b) 500 nm long SiNWs after the first oxidation (dry oxidation, 975°C, 3.5 hr) and oxide release. The NW diameter (stem) is approximately 45 nm. The top portion in (a) was significantly narrower and bending was observed in the absence of the supporting oxide layer.

To further reduce the diameter, a second oxidation was needed. As the samples without the oxide layer had started to show some bending [Fig. 25(a)], the second oxidation must be performed on samples with oxide layer intact which serves as a support for the structure. The oxidation step (including the first and the second oxidation) for three such samples are summarised in Table 5.

Table 5. Oxidation conditions of ultra-thin SiNWs

Sample	1^{st} oxidation	2^{nd} oxidation
S1	Dry, 975°C, 3 hr 30 min	Dry, 875°C, 6 hr
S2	Dry, 975°C, 3 hr 30 min	Dry, 875°C, 8 hr
S3	Dry, 975°C, 3 hr 30 min	Dry, 875°C, 10 hr

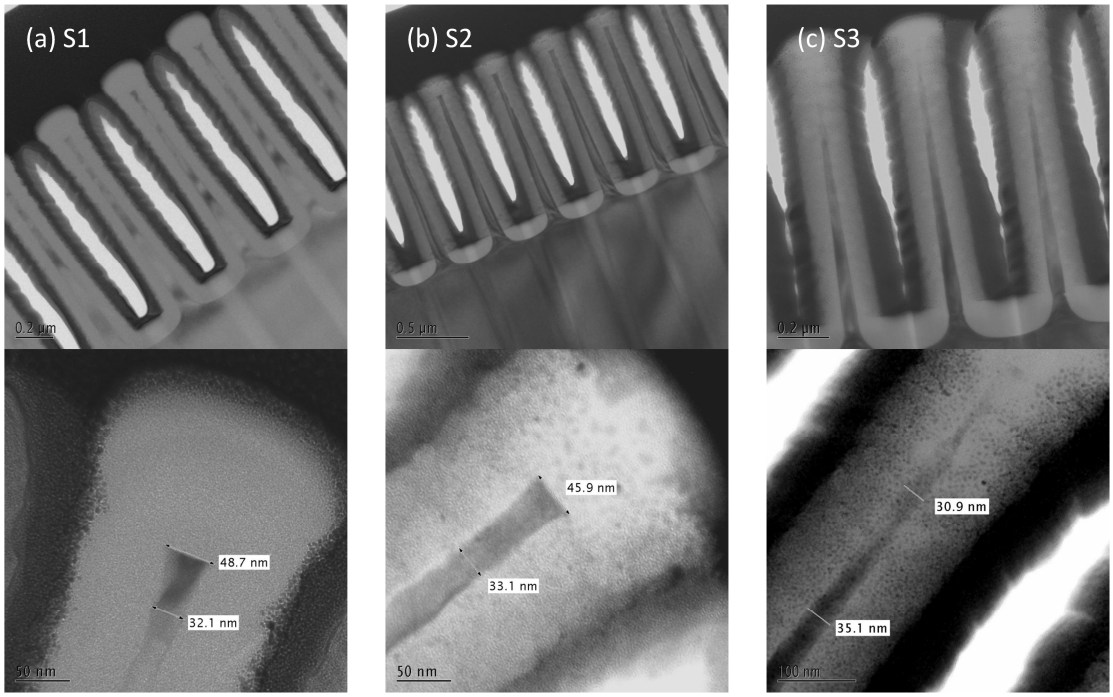

Fig. 26. TEM images of samples (a) S1 (b) S2 and (c) S3 after the second oxidation.

However, the effectiveness of the second oxidation is very limited. As observed from the Transmission Electron Microscope (TEM) images, the NW diameters were still in the order of 30-40 nm (Fig. 26), only slightly reduced compared to the first oxidation. This could be attributed to the low oxidation rate of the diffusion limited process in the presence of a thick oxide layer.

7.2 Results and discussion

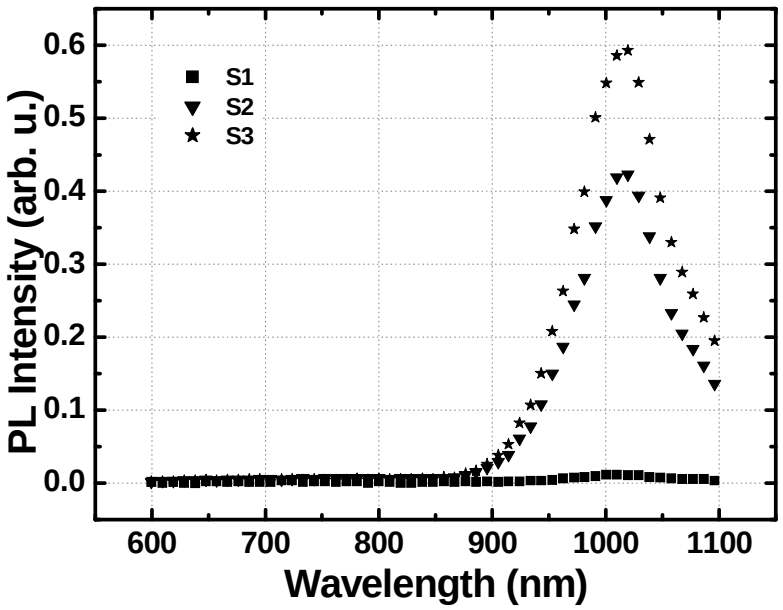

Fig. 27. PL signals of samples S1-S3.

Samples after the second oxidation were excited by laser at wavelength of 532 nm and PL signals were recorded (Fig. 27). The amplitude of PL intensity increases as the NW diameter is scaled down. While PL for sample S1 (diameter ≈ 45 nm) is negligible, sample S2 (d ≈ 40 nm) and S3 (d ≈ 33 nm) show visible PL spectral response, with a peak at approximately 1020 nm, which is situated close to the band gap of bulk silicon (1108 nm). The slight blue shift might be attributed to recombination centres at the Si/SiO_2 interface within the forbidden band of bulk Si, which contribute to the band gap lowering.

For ultra-thin nanostructures, there would be significant blue shift of the PL peak signal from the bulk Si band gap due to quantum confinement effect [36]. However,

this effect is not observed from the PL signals of our samples as their dimension still lies within the bulk region.

Therefore, to obtain sufficiently high PL signal for time-resolved analysis, the diameters of the SiNWs need to be further reduced to quantum confinement level. Meanwhile, passivation techniques such as hydrogen passivation [36] of the wires might help to improve surface condition of the wires and to reduce recombination centres at the Si/SiO_2 interface [35].

CHAPTER 8

FUTURE DEVICE DESIGN

8.1 Device structure

A new device structure is proposed and illustrated in Fig 28, based on the literature reviews and experimental studies done in this work.

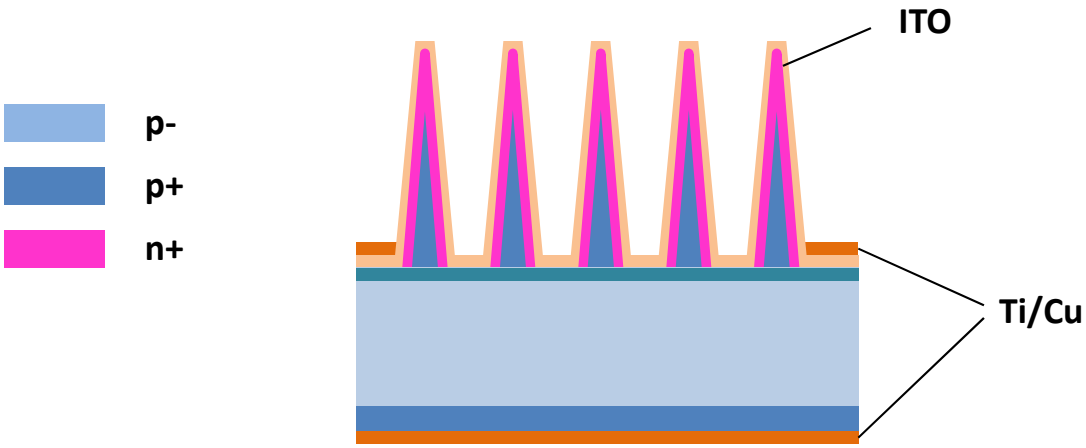

Fig. 28. Schematic diagramme of the proposed future SiNW PV device

The proposed device aims at utilising the orthogonalisation of carrier generation-transport in core-shell SiNW device (Chapter 6) and harvesting the effect of MEG (Chapter 7). In consists of a p- type Si substrate with BSF, and an array of tapered SiNWs covered on the top surface. The tips of the tapered SiNWs were reduced to the order of sub 10 nm in order to activate MEG. Core-shell radial p-n junctions are formed within the SiNWs, to facilitate efficient carrier transport.

Carrier collection process could be further optimised by depositing a layer of transparent conducting film such as indium tin oxide (ITO) onto the top nanostructures as front electrode. This could avoid problems associated with poor gap

filling of metal sputtering and possible damage to the ultra-thin nanotips if metal electrode is used. Meanwhile, shadowing loss of light generated current discussed in Chapter 5 and 6 could also be minimised, as non-transparent metal grids are now not located at the surface of nano arrays, leaving the nanostructures fully exposed to solar irradiation.

CHAPTER 9

CONCLUSION

In this work, the prospect of using SiNWs as a modification to the conventional single junction crystalline Si solar is researched and explored. SiNWs present numerous advantages as compared to conventional bulk structure in PV device applications, the most prominent among which are anti-reflection property, decoupling of light absorption and carrier separation, impurity tolerance and possibility of multi-exciton generation (MEG).

Some of the SiNW PV devices fabricated and reported by various groups have been studied. Although the measured power conversion efficiencies (PCEs) are still limited to less than 10%, it is believed that the modification on certain technical issues such as nanowire diameter optimisation and surface passivation will yield significant improvement on device performance.

Experimental studies have been carried out to fabricate both buried and core-shell p-n junction SiNW device. Optical reflectance measurements display excellent anti-reflection properties of Si nanostructures, while I-V characterisations demonstrate significant improvement in light generated current by orthogonalisation of carrier generation and transport. Although the overall PCEs of SiNW based devices are limited by relatively low fill factors, a further analysis into series resistance shows that upon reducing the effect of R_s, PCE of the devices could be notably improved.

In addition, samples with SiNWs surrounded by thermal SiO_2 have been made to investigate the light-emitting property, which is a precursor for MEG detection in SiNWs. Two of the three samples show visible photoluminescence (PL) peak close to

bulk Si band gap with a slight blue shift which could be attributed to recombination centres at Si/SiO_2 interface. This result confirms PL as a reliable measure of exciton generation in SiNWs, thus implying that time-resolved PL (TRPL) as a MEG detection method in Si nanocrystals could also be adopted in MEG studies of SiNW. No MEG is observed in this experiment as the nanowire dimension is still in the bulk region. To demonstrate MEG in SiNWs, wire diameters need to be further reduced to sub 10 nm levels by thermal oxidation.

Finally, a new device design has been proposed based on literature and experimental studies. The structure is similar to that of a core-shell SiNW based device, with the tips of SiNWs reduced to less than 10 nm. By adopting a radial p-n junction with a sub 10 nm tip in the nanowires, the short-circuit current density can possibly be further improved by the combined effect of efficient carrier generation-collection process in core-shell SiNWs and MEG effect in ultra-thin nanotips.

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